DEVELOPMENT OF HIGH FREQUENCY POWER CONVERSION TECHNOLOGIES FOR GRID INTERACTIVE PV SYSTEMS

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ABSTRACT

This thesis examines the development of DC-DC converters that are suitable for Module Integrated Converters, (MICs), in grid interactive photovoltaic (PV) systems, and especially concentrates on the study of the half bridge dual converter, which was previously developed from the conventional half bridge converter.

Both hard-switched and soft-switched half bridge dual converters are constructed, which are rated at 88W each and transform a nominal 17.6Vdc input to an output in the range from 340V to 360Vdc. An initial prototype converter operated at 100kHz and is used as a base line device to establish the operational behaviours of the converter. The second hard-switched converter operated at 250kHz and included a coaxial matrix transformer that significantly reduced the power losses related to the transformer leakage inductance.

The soft-switched converter operated at 1MHz and is capable of absorbing the parasitic elements into the resonant tank. Extensive theoretical analysis, simulation and experimental results are provided for each converter. All three converters achieved conversion efficiencies around 90%. The progressive increases in the operation frequency, while maintaining the conversion efficiency, will translate into the reduced converter size and weight. Finally different operation modes for the soft-switched converter are established and the techniques for predicting the occurrence of those modes are developed. The analysis of the effects of the transformer winding capacitance also shows that soft switching condition applies for both the primary side mosfets and the output rectifier diodes.

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LIST OF SYMBOLS

B	Parameter used to determine the boundary condition
C_1, C_2	Equivalent resonant capacitance
C_{a1}, C_{a2}	Additional resonant capacitance
C_D	Driving circuit capacitance
C_{DT}	Driving circuit oscillation capacitance
C_o	Output capacitance
C_{oss}	Mosfet output capacitance
C_s	Snubber capacitance
C_T	Transformer primary secondary capacitance
C_W	Transformer winding capacitance
D	Switch duty cycle
$\hat{E}$	Maximum input voltage
E	Input voltage
f_s	Switching frequency
i_D	Diode current
i_L	Inductor current
i_{Lr}	Resonant inductor current
i_o	Output current
i_Q	Mosfet current
i_S	Input current
I	Average output current
I_0	Average current in the input inductor L_1 or L_2

I_D	Mosfet drain current rating
I_F	Diode forward current rating
I_{op}	Peak output current
k	Load factor
k_Δ	Penetration depth coefficient
l_w	Total winding length
L_a	Additional resonant inductance
$L_{coaxial}$	Coaxial transformer leakage inductance
$L_{leakage}$	Transformer leakage inductance
L_r	Equivalent resonant inductance
n	Transformer turns ratio
N_s	Number of secondary turns per primary turn in the coaxial winding
$\hat{P}$	Unit power loss in transformer primary secondary capacitance
P_{CT}	Power loss in transformer primary secondary capacitance
r_{pi}	Inner radius of the outer conductor in the coaxial winding
r_s	Outer radius of the inner conductor in the coaxial winding
R	Load resistance
R_D	Driving circuit resistance
R_{DT}	Driving circuit oscillation resistance
$R_{DS(on)}$	Mosfet drain source on resistance
t_{rr}	Diode reverse recovery time
T_s	Switching period
v_{C1}, v_{C2}	Resonant capacitor voltage
v_{CT}	Voltage across transformer primary secondary capacitance

v_{CW}	Voltage across transformer winding capacitance
v_D	Diode voltage
v_Q	Mosfet voltage
v_S	Transformer secondary voltage or rectified transformer secondary voltage
v_T	Transformer primary voltage
$\hat{V}$	Unit voltage across each output voltage doubler capacitor
V	Average output voltage
V_d	Output capacitor voltage reflected to the transformer primary
V_{dc}	Capacitor rated dc voltage
V_{DS}	Mosfet drain source voltage rating
V_F	Diode forward voltage drop
V_{RRM}	Diode repetitive peak reverse voltage rating
V_Z	Nominal zener voltage
Z_0	Characteristic impedance
Δ	Penetration depth
Δ_1	Initial current coefficient
Δ_2	Initial voltage coefficient
μ_0	Permeability of free space
ω_0	Angular resonance frequency

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DECLARATION

I hereby declare that the main text in this thesis is an original work of the author and no part has been used in the award of another degree.

_____

Quan Li

PUBLICATIONS

The following publications have been produced during the course of this thesis.

[i] Q. Li, P. Wolfs and S. Senini, "The Application of the Half Bridge Dual Converter to Photovoltaic Applications," Proceedings of Australasian Universities Power Engineering Conference, 2000, pp. 156-161. International Journal of Renewable Energy Engineering, Vol. 3, No. 3, pp. 367-372, 2001.

[ii] Q. Li and P. Wolfs, "Half Bridge Dual Converter with a Coaxial Matrix Transformer," Proceedings of Australasian Universities Power Engineering Conference, 2001, pp. 257-262.

[iii] Q. Li and P. Wolfs, "A Resonant Half Bridge Dual Converter," Proceedings of Australasian Universities Power Engineering Conference, 2001, pp. 263-268. Journal of Electrical & Electronic Engineering Australia, Vol. 22, No. 1, pp.1-7, 2002.

[iv] P. Wolfs and Q. Li, "An Analysis of a Resonant Half Bridge Dual Converter Operating in Continuous and Discontinuous Modes," Proceedings of IEEE Power Electronics Specialists Conference, Cairns, Australia, June 2002.

1. INTRODUCTION

This thesis concentrates on the development of a DC-DC converter topology that has potential applications in photovoltaic (PV) systems, especially module integrated converter systems. Chapter one will review the photovoltaics industry and establish the interest in module integrated converter technology shown in the recent literatures. Chapter two makes a study of MIC technology, identifies a suitable topology and reviews the typical design solution. Shortcomings in this solution are identified. Chapter three discusses the half bridge dual converter as a promising alternative. Chapters four and five then describe the development of prototype converters based on this approach. Much of the work contained in these chapters has appeared in the 2000 and the 2001 AUPEC conferences. These chapters present several important advances including the application of matrix and coaxial transformer techniques and the development of a new resonant converter based on the half bridge dual topology. A systematic evaluation of loss mechanisms allows the converter frequency to progressively increase from 100kHz to 250kHz and finally 1MHz for the resonant designs. The conclusions summarize the achievements of the thesis and identify areas of future work.

1.1 World Usage of Photovoltaic Energy

To combat the worldwide shortage of conventional energy, especially in the developing nations, more and more research work has been focused on the

renewable energy technologies. Compared with the conventional energy, renewable energy has the following advantages:

- It is self-renewing or non-depletive. This fact is readily known by its definition.
- The sources are abundant. The availability of renewable energy each day is far more than what is released by all fossil fuels consumed, [1].
- It does less damage to the environment. Renewable energy applications generate less greenhouse gases, which could severely damage the Earth's climate.
- The operational cost, in the long term, is low, because high environmental clean-up cost is avoided.

Among all the renewable energy sources, PV energy perhaps has the greatest potential. Within one minute, the total energy reaching the Earth from the Sun outweighs the energy consumed by the world in one year, [2]. Without any rotating parts or emissions in the PV system, it is deemed as the simplest to operate. An emerging idea is to restructure the electricity supply networks by decentralizing the power generation. PV applications are suited to this role, [3]. Undoubtedly, PV energy will ultimately become a major competitor of the traditional energy sources.

PV energy has been used in the aerospace technology for about fifty years since the first practical solar cell was developed at Bell Laboratories, [4]. However, a broader use of PV energy took place only in the early 1970s. Thirty years of research has

proved PV energy one of the most promising renewable energy sources and brought a sharp increase of PV usage. Although the world's energy market is still dominated by conventional power systems, the total sales of PV energy in 2000 reached 288MW, which was 43% higher than in 1999, [1].

Even though the cost of PV has been falling at about 5% annually over the past twenty years, [5], the generation cost of PV energy is still very high, compared with the cost of the traditional electricity sources. In 2000, the cost of one Megawatt-hour generated from PV energy was about 200 Australian dollars, which is seven times that of the conventional coal fired power. This cost is even higher than other renewable energy sources such as wind energy, hydro power or biomass, [6]. Another important obstacle for using PV energy in a larger scale is the conversion efficiency. Currently, the efficiencies of most of the PV modules fall in the range of 10-20%, [7], although a record-breaking solar cell efficiency of 34%, built by Spectrolab Inc., has been reported, [8]. Further development of PV technology aims at accelerating the trend in reducing the generation cost and improving the efficiency.

1.2 Stand Alone and Grid Interactive Systems

There are two popular means to utilize PV energy: stand alone systems and grid interactive systems, which are respectively shown in Figures 1.1 and 1.2.

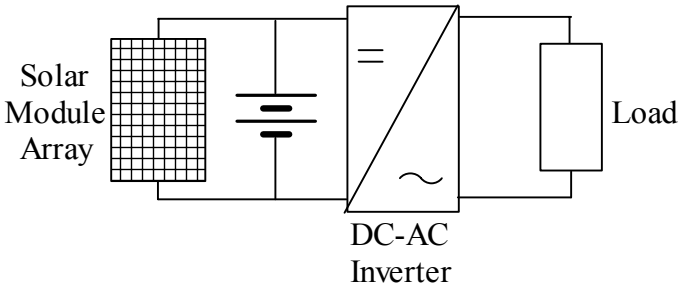


Figure 1.1 Stand Alone PV System

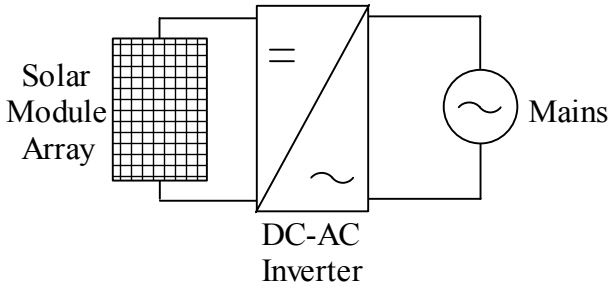


Figure 1.2 Grid Interactive PV System

In Figure 1.1, the dc voltage produced by solar arrays is inverted to the ac voltage and applied directly to the domestic load. A standard stand alone system usually consists of the following basic components:

- the PV module, which produces dc voltage,
- the inverter, which inverts dc power to ac power,
- the control module, which provides control to the whole system,
- a storage battery, which acts as a backup dc power source, and
- the cable that connects the PV module, the inverter, the control module and the storage battery.

The stand-alone system is more suitable for power supplies in remote areas, where no electric power grid is available.

In Figure 1.2, the dc voltage produced by solar cells is inverted to the ac voltage and connected to the grid. In the grid interactive system, the storage battery can be removed from the system, as the grid can provide a backup during the PV interruptions, [9]. Therefore, the cost of the whole system is lowered and the energy generated by PV modules is used to the greatest extent. Additionally, because the lifetime of the PV modules is over twenty years and that of the battery is significantly lower, the lifetime of the complete PV system is extended at no other costs. These important advantages of the grid interactive PV system make it a more viable solution to utilize the PV energy, especially when long public grids exist and the transmission costs are high.

Over the past few years, the fastest growing share of PV applications is the grid interactive section, which has grown from 4% in 1990 to 48% of the total world sales in 2000, [10]. In those countries with strong government support such as Germany, the portion of the grid interactive PV is even higher and already accounted for 83% of the total PV applications in 1998, [11]. This simply means that grid interactive PV will finally become the mainstream of the PV market.

1.3 Possible Arrangements for Grid Interactive Systems

Grid interactive systems can make use the following two technologies:

- Solar module arrays with a centralized grid interactive inverter, [12]. It is illustrated in Figure 1.3.
- Solar modules with panel sized inverters, or module integrated converters (MICs), [12]. It is illustrated in Figure 1.4.

The first technology is more conventional. Usually, this system tends to be reasonably large to achieve a low construction and operation cost. As the central inverter is used to interface a number of solar modules, this technology may have an advantage that only a small number of inverters are needed in a large PV system. However, the trade-offs of this design include:

- The cabling design has to be relatively complex in order to reduce the risk of dc arcs due to the high dc voltages and to overcome the high conduction loss due to additional diodes used in the system.
- The failure of the central inverter would remove all connected PV modules from service.
- Expanding an installed system is not possible without redesigning of the central inverter, [13].

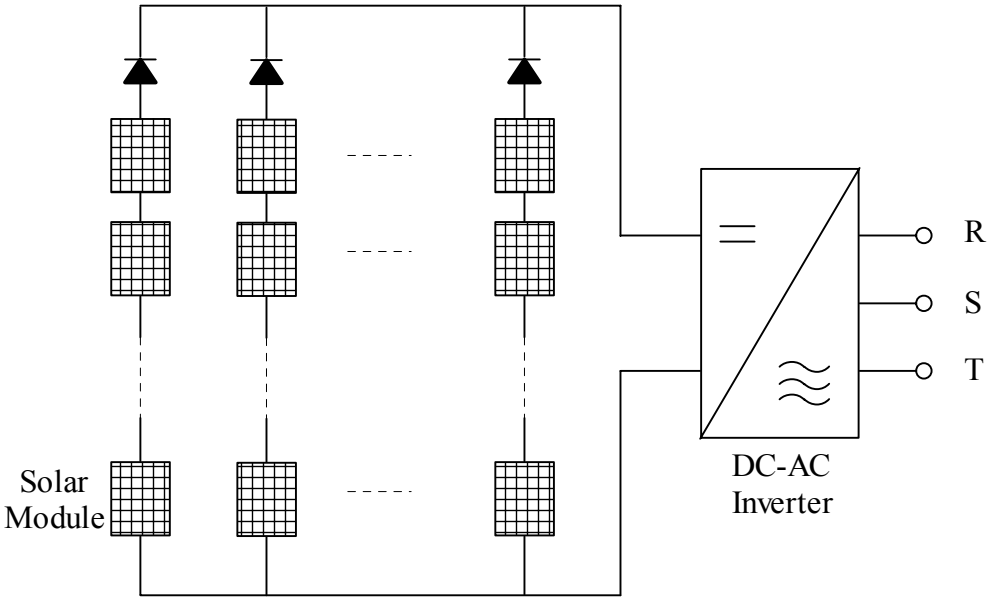


Figure 1.3 Grid Interactive System with a Central Inverter

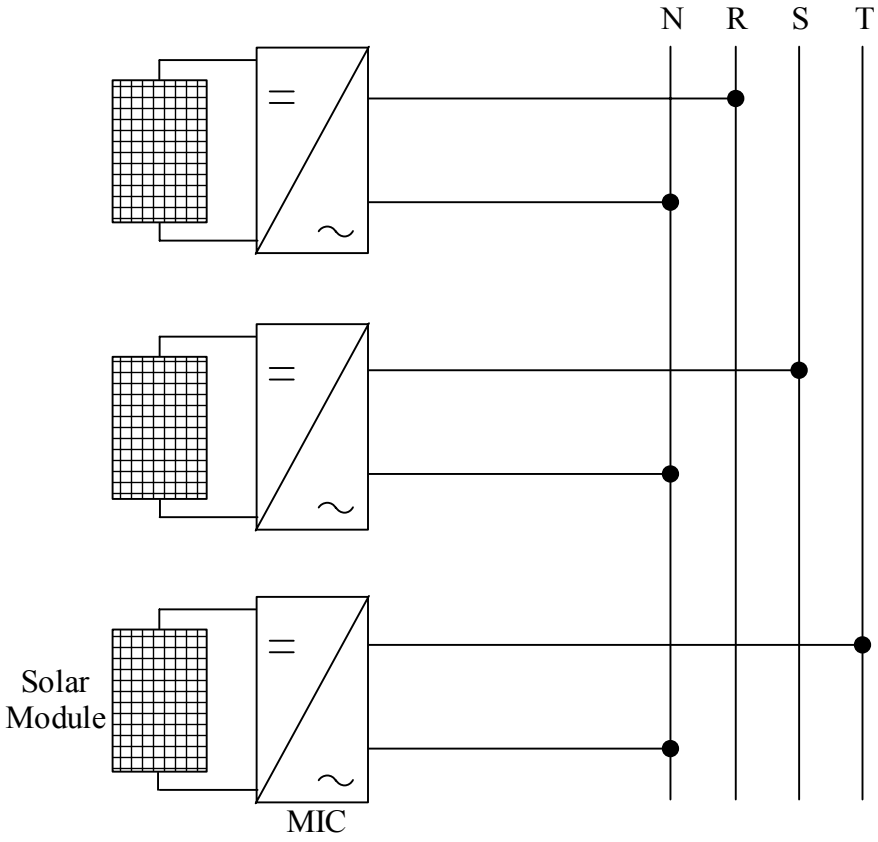


Figure 1.4 Grid Interactive System with MICs

The MIC technology makes the expansion of PV systems much easier. This explains why this technology has become more and more popular in PV applications in recent years. In this technology, each PV module has its own inverter and provides an ac output compatible with the mains voltage. The main advantages include:

- The need for costly dc cabling design is eliminated.
- The conduction loss is reduced due to a relatively higher ac voltage provided by each MIC.
- The failure of the individual inverter can only remove one connected PV module. This feature is very helpful in increasing the reliability and the performance of the complete system.
- System expansion can be realized by simply adding more PV modules, depending on the system requirement.

The MIC technology exploits highly modularized devices so that mass production can be employed to achieve a reduced construction and operation cost, [14]. Therefore, in both of the economic and the technical respects, grid interactive PV becomes a more feasible alternative source of renewable energy in comparison to the traditional electric power. The MIC technology will be examined in detail in the next chapter.

2. MODULE INTEGRATED CONVERTER IN PHOTOVOLTAIC APPLICATIONS

MICs for PV applications are usually integrated directly with the frame of the solar module and exposed to the extreme outdoor environmental conditions. Additionally, the solar module should be galvanically isolated from the mains. Therefore, a MIC, typically with the power rating of around 100 Watts, must fulfil the following basic requirements:

- high power-packing density,
- small volume and weight,
- high efficiency,
- reasonable life time and cost,
- high reliability, and
- isolation between the mains and the solar module.

2.1 Module Integrated Converter Topologies

There are two possible implementations for a MIC. Figure 2.1 shows a MIC made up of a converter and a 50Hz transformer. However, since 50Hz transformers with the power rating of around 100W generally have poor efficiencies and tend to be large and heavy, this implementation is not likely to be useful in PV applications.

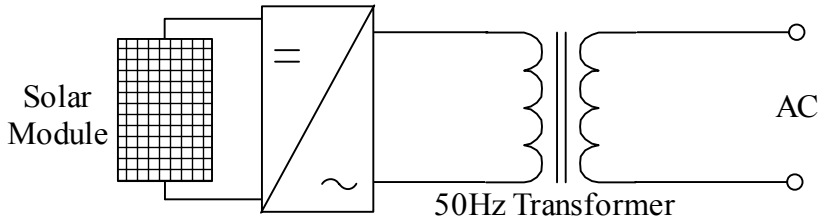


Figure 2.1 MIC with a 50Hz Transformer

The other implementation made up of two converters and a high frequency transformer is illustrated in Figure 2.2. By introducing a high frequency transformer, the size and weight of the complete device can be greatly reduced, [15]. In this implementation, the MIC performs two series power conversion steps: the dc power produced by solar cells is first converted to high frequency ac power and then converted back to 50Hz ac power.

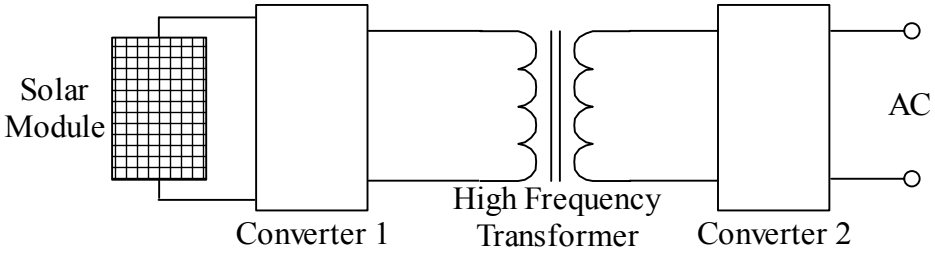


Figure 2.2 MIC with a High Frequency Transformer

The power conversion in the MIC with high frequency transformers can proceed in several different topologies. Solution A shown in Figure 2.3 is made up of one converter and one frequency changer, [16]. The dc power is first transformed to the high frequency ac power and then transformed to the mains frequency through the frequency changing converter. Figure 2.4 shows Solution B with two converters. In

Solution B, the solar module dc voltage is converted to a high level dc voltage, which allows direct inversion to ac voltage through the DC-AC inverter, [17]. Solution C is given in Figure 2.5. It is made up of one converter and one unfolder, which converts the folded waveforms to sinusoidal waveforms, [18].

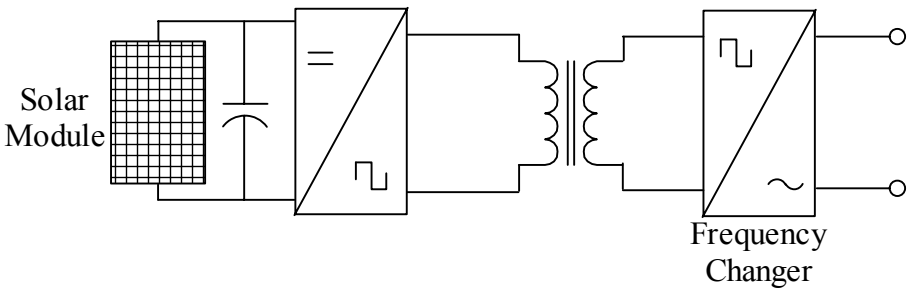


Figure 2.3 Solution A of MIC

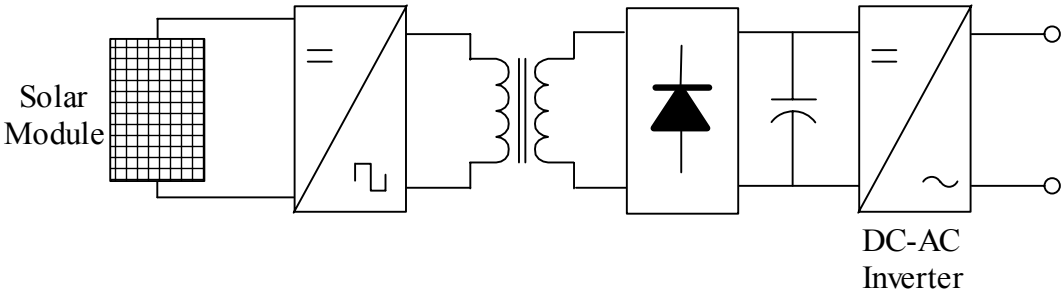


Figure 2.4 Solution B of MIC

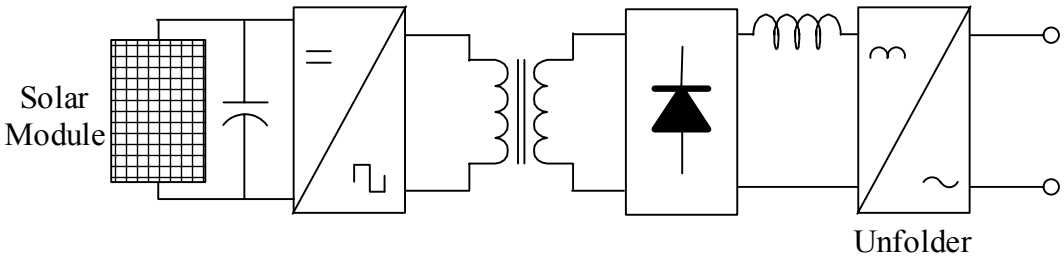


Figure 2.5 Solution C of MIC

All of these solutions require 100Hz power storage as they provide power to single phase loads. The capacitor is normally one of the largest components and a significant contributor to failure rates. Therefore, the selection of large electrolytic capacitors must be avoided in the converter stage to minimize the size and extend the lifetime of the MIC.

Solution B has an advantage in capacitor size. The power stored in a capacitor is proportional to CV^2 and the volume of a capacitor is proportional to CV, where C is the capacitance and V is the voltage across the capacitor. Apparently, the power density for a capacitor is proportional to V. Since the dc voltage is the highest in Solution B, the capacitor in this solution has the highest power density and for the same amount of power, has the smallest volume.

Moreover, Solutions A and C have more input stage operating stress. Because 100Hz power storage is at the solar module, the transformer and primary converter have fluctuating loadings and must be designed to handle peak powers which are up to twice the average load power. Another disadvantage is the complex design of the frequency changer in Solution A. Therefore, Solution B may be the best choice for MIC topology in PV applications.

2.2 DC-DC Converter Features

In Solution B for MIC implementations discussed above, the key component is the DC-DC converter. In some cases such as remote area power supplies,

uninterruptible power supplies and computer power systems, DC-DC converters must have four-quadrant operation ability to allow power to be transferred from ac side to dc side, [19]. However, this is not true in grid-interactive PV systems, where no storage battery exists. Therefore, this thesis will concentrate on the single-quadrant DC-DC converters.

The DC-DC converter in a MIC performs the following functions:

- Transformation of dc voltage from one level to another,
- Regulation of the dc output voltage against input and load variations, and
- Provision of isolation between the input and the output.

Along with constant demands for high-performance, small-volume power sources, many DC-DC converters have been developed, [20]. Most of the widely used DC-DC converters have evolved from the basic buck or boost converters. The operations of a basic buck converter and a basic boost converter are described in Appendix 1.

The absence of a physical dc transformer is one of the reasons for building a DC-DC converter. Compared with the traditional 50Hz ac transformer, the DC-DC converter has two important merits. One is its high power-packing density. The DC-DC converter works at high frequency and the energy transferred in each individual period is low. Consequently, the size of the transformer can be reduced and the selection of small inductors and capacitors in the filter network can be

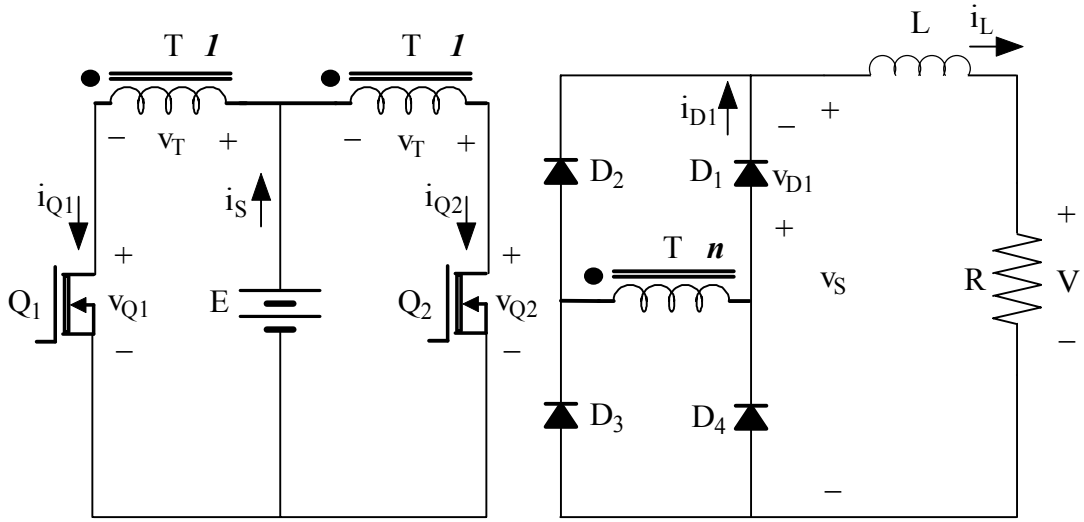
achieved. This feature makes small volume and light weight designs possible. The other merit is its high efficiency. The switching semiconductors in the DC-DC converter work in the saturation area rather than the active area. Ideally, the voltages across the switching semiconductors are zero when they are closed and the currents through them are zero when they are open. No power loss is associated with the switching semiconductors. Therefore, in the converter with ideal switches, all input power is absorbed by the load and the efficiency is 100%. However, this cannot be easily achieved by linear dc power supplies, where a significant part of power is dissipated in semiconductor devices. Additionally, this second feature also makes a large heat sink unnecessary for the DC-DC converter and helps in gaining a compact design.

2.3 The Push-Pull Converter

In PV systems, the dc voltages supplied by the solar cells tend to be low. Therefore, DC-DC converters with a high performance under low input voltages are desirable. To date, the most common DC-DC converter for photovoltaic applications, which has a typical power rating of around 100 Watts, would have been the center tapped push-pull converter. The operation of this converter will be examined to provide a point of reference for other converter comparisons. Figure 2.6 shows its circuit schematic and waveforms.

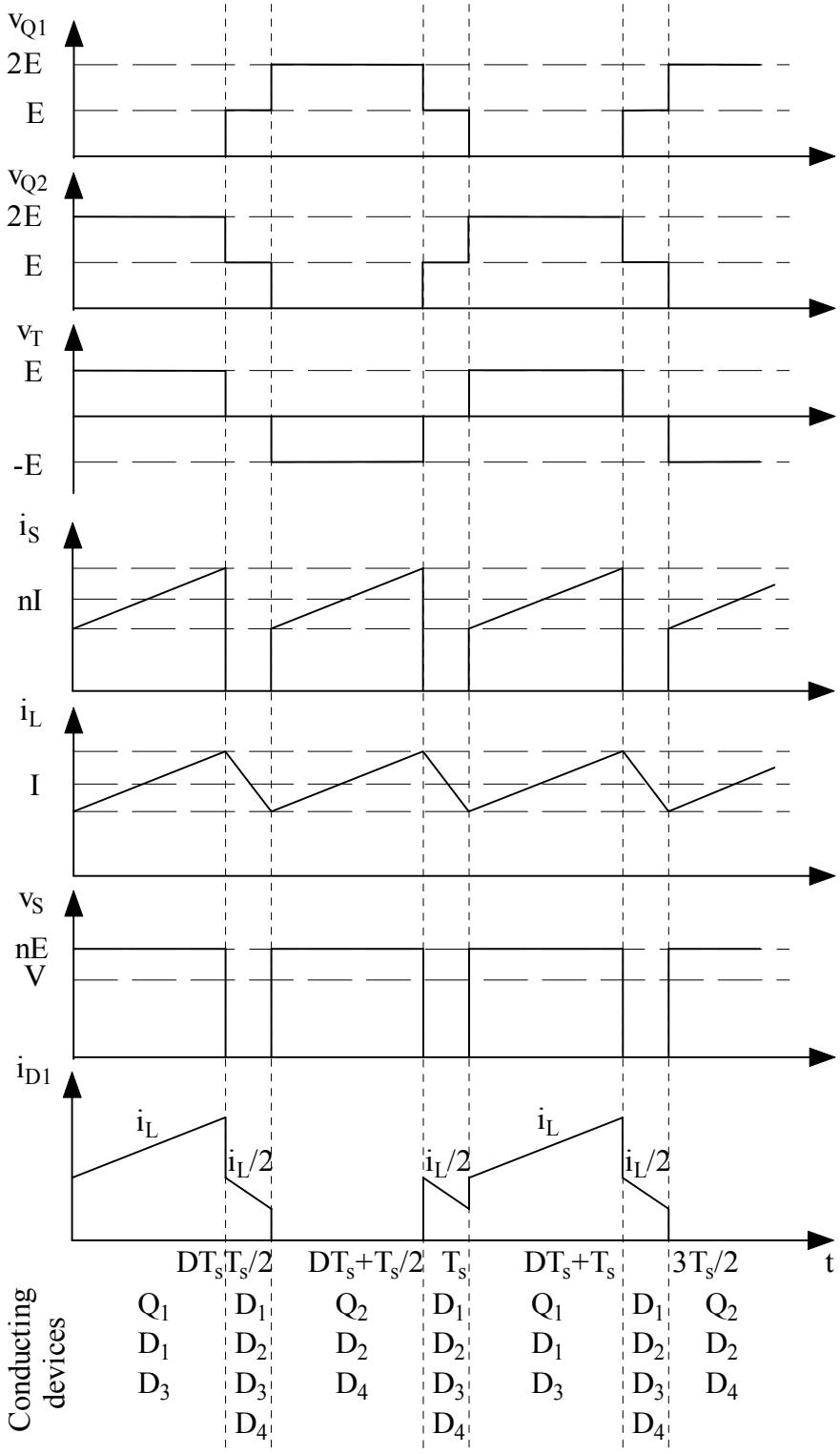
The maximum duty cycle of the push-pull converter is slightly less than 50%. Otherwise, “shoot-through” will take place in the two switching semiconductors. To

avoid the “shoot-through”, a dead time, which is at least equal to the turn-off time of the switching semiconductors, must be inserted between the turn-off of one switch and the turn-on of the other. The operation of the converter can be divided into three stages. When Q_1 is closed and Q_2 is open, the input voltage is applied, dot negative, to the transformer primary winding. When Q_2 is closed and Q_1 is open, the input voltage is applied, dot positive, to the transformer primary winding. During these two stages, the input power is transferred to the output load and the converter is said to be in the powering stage. When both of the switches are open, the current in each of the primary windings is zero and the converter is said to be in the buck stage.



(a)

Figure 2.6 The Push-Pull Converter (a) Circuit



(b)

Figure 2.6 The Push-Pull Converter (Continued) (b) Waveforms

The push-pull converter is a buck derived converter. According to the principles shown in Appendix 1 and the existence of the transformer, the output voltage can be calculated to be

$$V = 2n \cdot D \cdot E \tag{2.1}$$

where n is the transformer turns ratio and D is the duty cycle of each switch.

In the center tapped push-pull converter, the peak switch voltage is twice the maximum input voltage and the peak switch current is equal to the peak input current, if the additional voltage and currents stresses resulting from the circuit parasitic components are not considered. This characteristic offers an advantage in PV applications, where the dc voltages supplied by solar cells tend to be low. Other advantages of the push-pull converter include:

- Can operate with reasonable primary to secondary leakage inductance. The energy stored in this inductance is recovered in normal operation.
- Provides self-clamping of switch off state voltage to twice of the input voltage, if the primary winding halves have negligible leakage.

However, the performance of the push-pull converter under a large input voltage range is not satisfying. This can be seen from the following example, where the input voltage E varies from $0.5\hat{E}$ to $\hat{E}$. Because the duty cycle has to be restricted

to slightly less than 50%, it will not help in increasing the gain and usually stays unchanged. In order to obtain a desired output voltage level, the transformer turns ratio must be designed for the lowest input voltage, $0.5\hat{E}$, that is, this ratio has to be doubled. Under the new ratio, when operating the converter under the input voltage of $\hat{E}$, the duty cycle D has to be halved to obtain the same level of the output voltage. Waveforms under different input voltages of $0.5\hat{E}$ and $\hat{E}$ are shown in Figure 2.7.

In Figure 2.7, n' = 2n and D' = D/2. Under the doubled transformer turns ratio, the duty cycle has to vary with different input voltages to keep the output voltage the same. But, this will give twice the peak switch current and twice the diode reverse voltage compared with the normal transformer turns ratio. It is an important disadvantage of this type of converter that higher ratings of switching devices and diodes are required under a wide range of input voltages.

Some possible disadvantages of the push-pull converter include:

- Requires low primary to primary leakage inductance – this would be a limiting factor on converter power rating.
- Has an issue with diode reverse recovery because it is the buck derived converter with an inductive filter.
- Presents higher primary peak current and lower copper utilisation at best 50% for the primary side.

- Transformer dc balance can be an issue, especially at higher ratings, [21].
- Incurs higher switch current stress and diode reverse voltage stress if a wide operating range of input voltages is required.

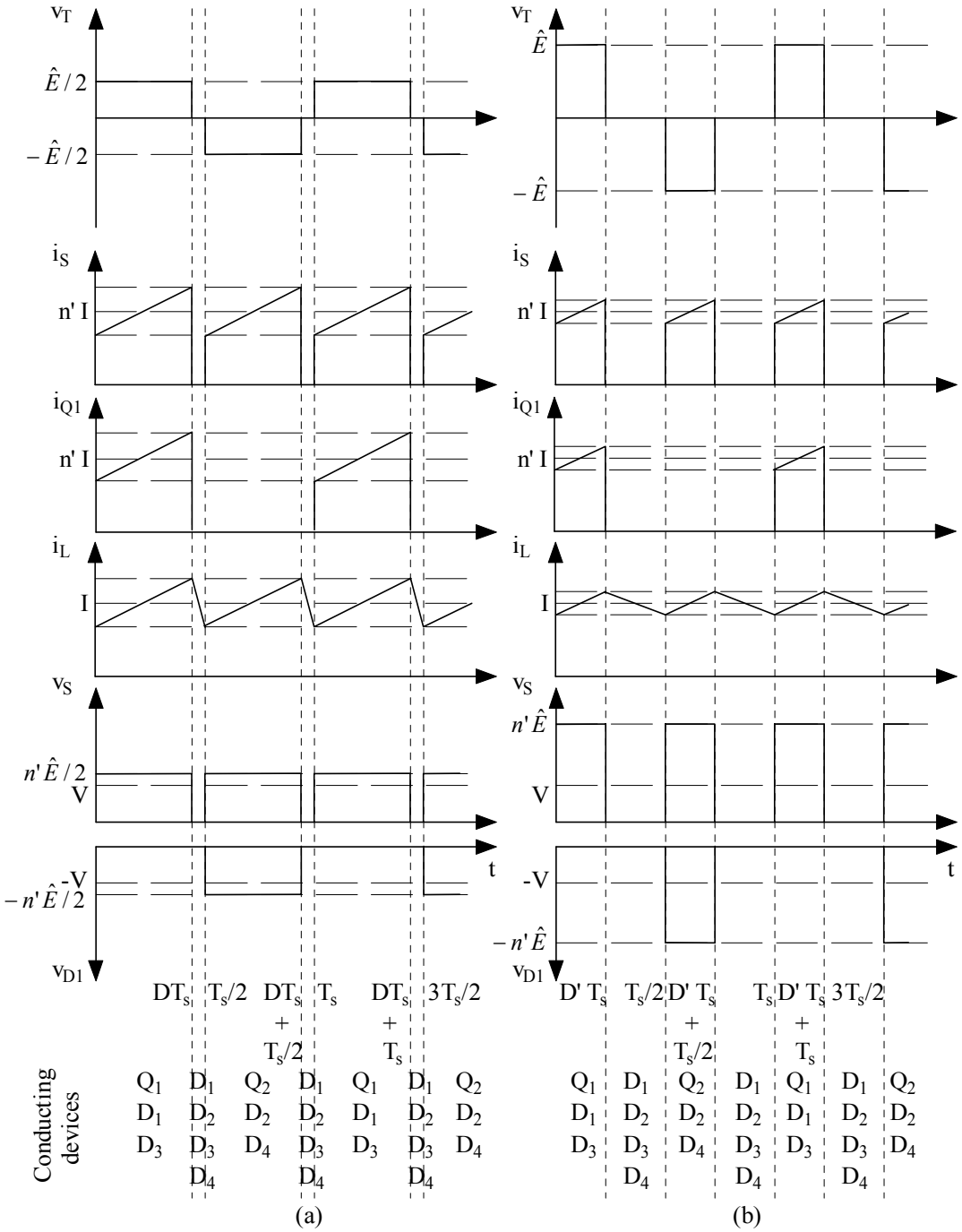


Figure 2.7 Waveforms under Different Input Voltages (a) E = 0.5 $\hat{E}$ (b) E = $\hat{E}$

2.4 Selection of a Converter Topology

The push-pull converter is widely used in low voltage applications. However, shortcomings do exist. A fundamental question is "Do better choices exist?" Standard texts on DC-DC converters offer some useful guidelines, [20]. These are:

- Direct buck or boost converters offer lower levels of device stress.
- Converters with symmetric excitation of the transformer offer better magnetic utilization.

These guidelines reduce the field considerably. Further preferences would include:

- A boost topology in terms of reduced output diode stress. In a boost converter, the capacitive output filter clamps the diode reverse voltage whereas in a buck converter the inductive filter generates excess reverse voltage due to diode reverse recovery. Diode snubbers are often required in a buck application where inductive filter is used, [22].
- A current fed transformer in terms of balance. A current fed transformer offers automatic volt-second balance while a voltage fed transformer tends to experience volt-second unbalance problems, [23].

- Full utilization of the transformer windings. Since transformers are normally one of the bulky components in DC-DC converters, full utilization of the copper windings simply means smallest transformer volume.
- Single switching devices in the primary current path, to limit conduction losses. Having more than one switch conduct in the primary current path incurs higher conduction losses due to the series connection of the switch forward resistances.
- An absence of "high side" switches, to avoid the painstaking work involved in designing a more complex driving circuit. If the switch is not connected to the main circuit ground, the driving circuit must also be floating in order to provide the correct gate signal.

These preferences are met by the half bridge dual converter – the central topic of this thesis.

3. THE HALF BRIDGE DUAL CONVERTER

This chapter will outline the properties of the half bridge dual converter and examine its suitability for MIC applications. Because the half bridge dual converter was previously developed from the more conventional voltage sourced half bridge converter using duality theory, [24], the operation of the half bridge converter will be explained first.

3.1 The Half Bridge Converter

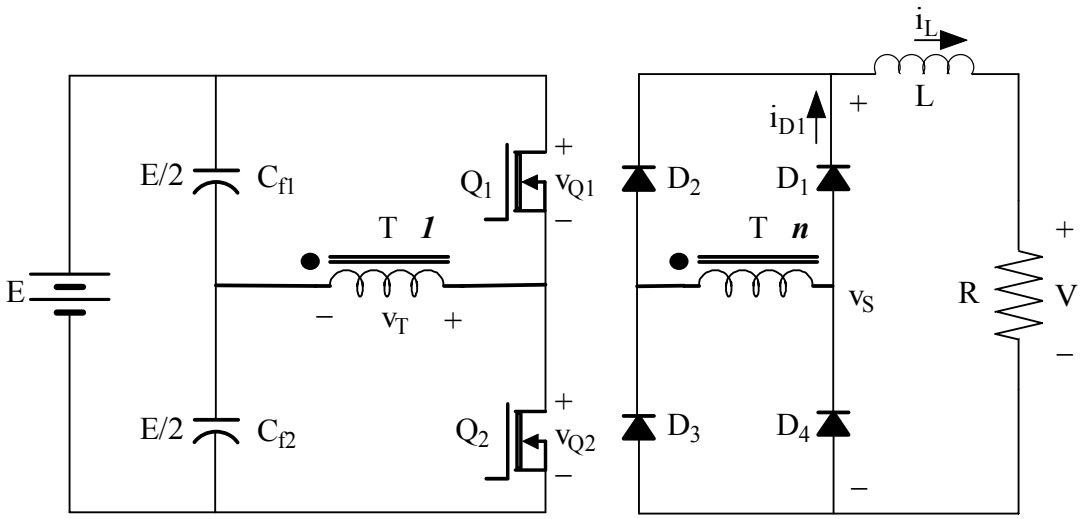
Figure 3.1(a) shows the circuit schematic of the half bridge converter, which is a buck derived converter. On the input side, capacitors C_{f1} and C_{f2} are series connected and the input voltage, E, is equally distributed between them. Two switches in the half bridge converter, Q_1 and Q_2, conduct alternatively and thus apply either +E/2 or –E/2 across the transformer primary. The alternating voltage on the secondary side is full-bridge rectified to a single-polarity voltage. An inductor is used as the filter in the secondary side to attenuate the ripple components in the current and provide the current stiff feature for the output. Similar to the push-pull converter illustrated in Chapter two, the maximum duty cycle for each switch in the half bridge converter should be less than 50%. Due to the switching transients such as the turn-off time of the switching semiconductors, a duty cycle of 50% or more will cause a short circuit of the input voltage source and this is destructive to the converter. Assuming that capacitors are big enough, the charging and discharging

currents will only cause negligible ripples in the capacitor voltages. Based on this assumption, the waveforms of the half bridge converter are shown in Figure 3.1(b).

Because the half bridge converter is buck derived, the principles of buck converters in Appendix 1 can be easily applied to it. Considering the existence of the transformer, the output voltage of the half bridge converter can be calculated to be

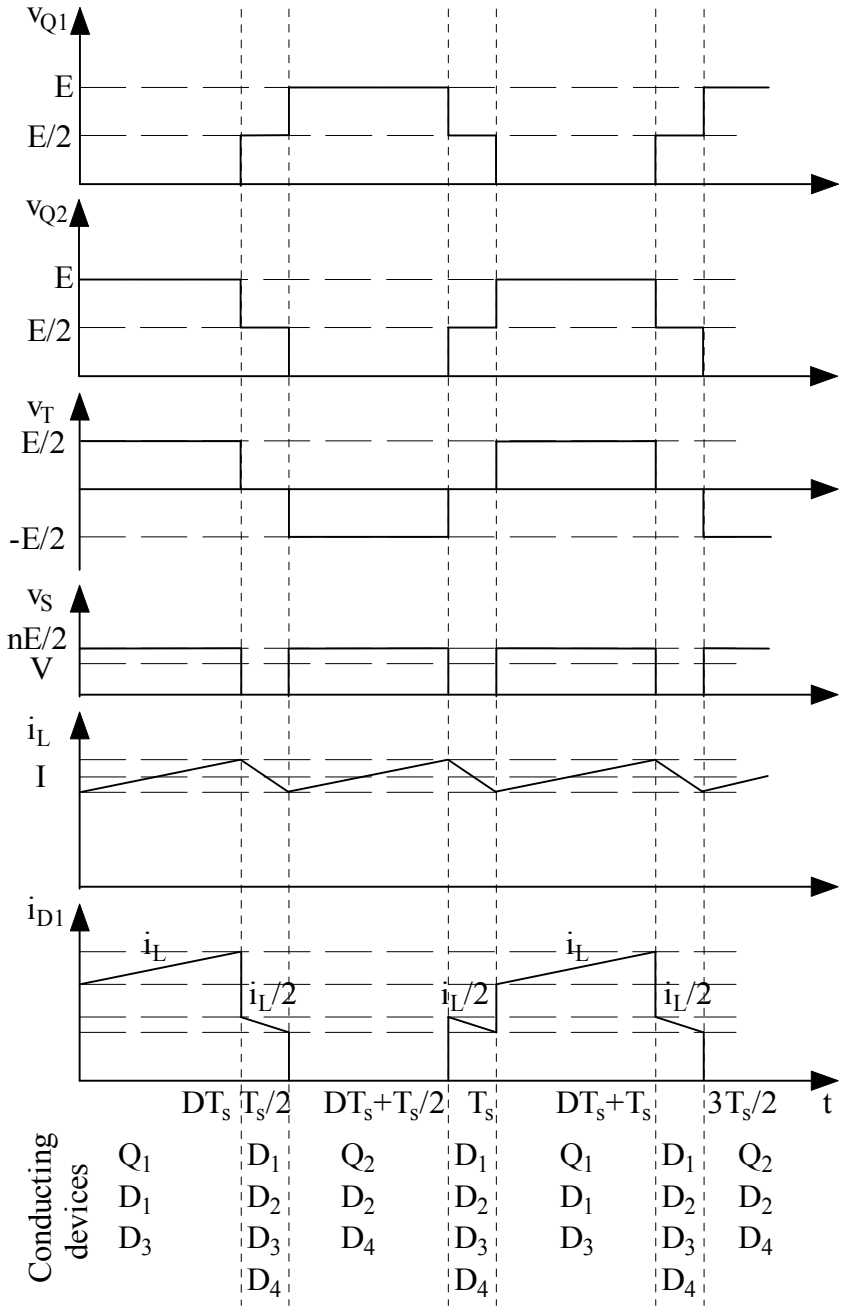
$$V = n \cdot D \cdot E \tag{3.1}$$

where n is the transformer turns ratio and D is the duty cycle of each switch.



(a)

Figure 3.1 The Half Bridge Converter and Its Waveforms (a) Schematic



(b)

Figure 3.1 The Half Bridge Converter and Its Waveforms (Continued) (b) Waveforms

One advantage of the half bridge converter is that the peak voltage across the switch is clamped to the input voltage. This feature is of interest when operating the

converter in high input voltages. However, the peak switch current would be at least twice the input current. Therefore, the half bridge converter is suited to the dc input source with a higher voltage and a lower current.

3.2 The Half Bridge Dual Converter

This thesis specifically examines the half bridge dual converter. The following texts will illustrate its topology, features and operation basics.

Figure 3.2 shows the circuit of the half bridge dual converter, as derived from the half bridge converter using the duality principle, [24]. Duality principle is widely known in the network theory. A network $\hat{N}$ is the dual of the network N if the following two requirements are fulfilled, [25]:

- The topological graph of $\hat{N}$ is the dual of the topological graph of N, where there is a one-to-one correspondence between the meshes and the nodes of the topological graph of $\hat{N}$ and the nodes and the meshes of the topological graph of N.
- The branch equation of a branch of $\hat{N}$ is obtained from its corresponding equation of N by changing v to $\hat{i}$, i to $\hat{v}$, q to $\hat{\phi}$, ϕ to $\hat{q}$, where v, i, q and ϕ are respectively the branch voltage, current, charge and flux for N, and $\hat{v}$, $\hat{i}$, $\hat{q}$ and $\hat{\phi}$ are the corresponding branch variables for $\hat{N}$.

The above techniques, together with the dual circuit models for transformers and ideal switches [26], offer the possibility to derive the half bridge dual converter shown in Figure 3.2.

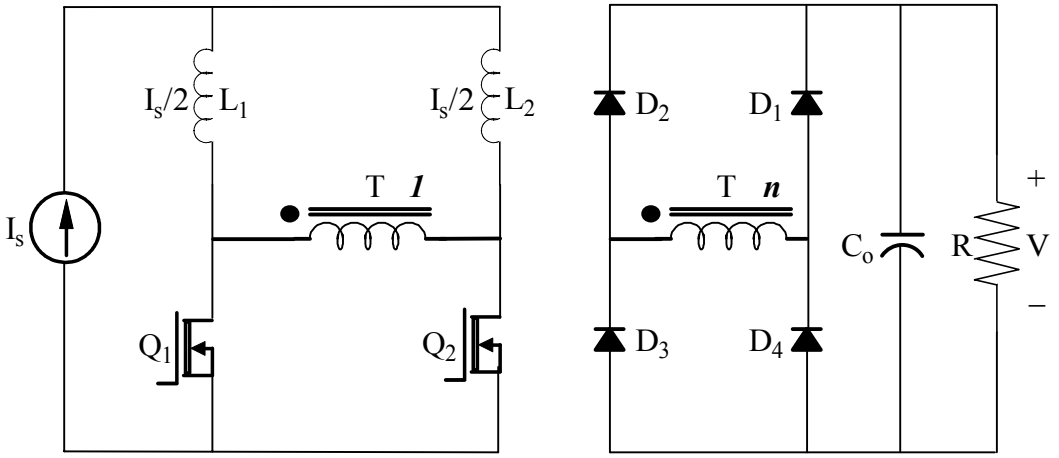


Figure 3.2 The Half Bridge Dual Converter

The half bridge dual converter is a boost-derived converter. On the primary side of the half bridge dual converter, one current source and two inductors replace the corresponding voltage source and capacitors in the half bridge converter. The input current, I_s, is shared equally between two inductors, L_1 and L_2. The alternative openings of two switches, Q_1 and Q_2, will direct either $+I_s/2$ or $-I_s/2$ through the transformer primary. On the output side, the full bridge rectifier is the same as in the half bridge converter. The only difference is that the filter consists of a capacitor instead of an inductor and is therefore voltage stiff. The maximum duty cycle for each switch in the half bridge dual converter, unlike that of the push-pull converter and the half bridge converter stated in the previous texts, should be larger than 50%. Otherwise, taking into the effect of the delay of the switches' turn on in the practical

operation, even 50% duty cycle might result in the openings of both switches. In this occasion, the current source is open-circuited, something which is intolerable. This event is the dual of the "shoot-through" feature of the half bridge converter.

Because the half bridge dual converter is the dual version of the half bridge converter, it has dual properties. Some important dual properties of the two converters are given in Table 3.1.

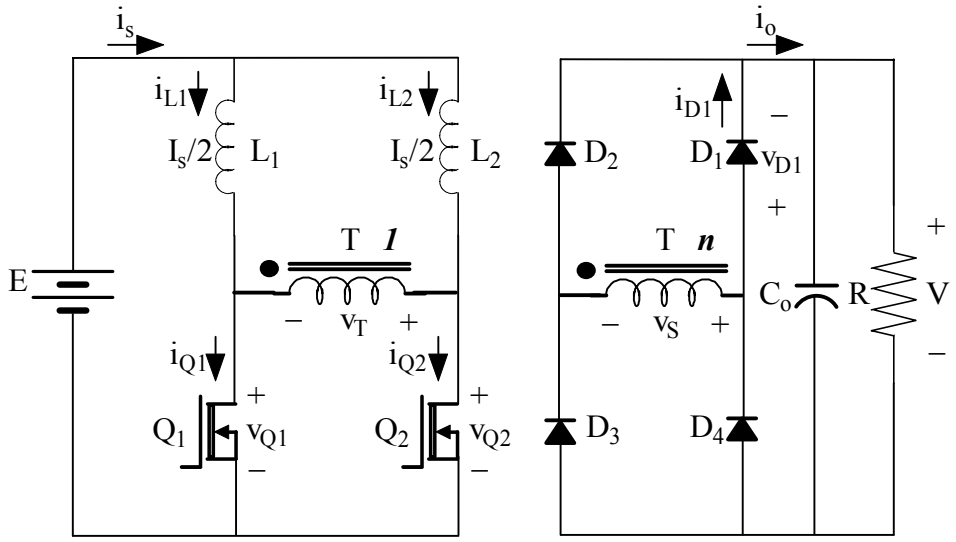
Half Bridge Converter	**Half Bridge Dual Converter**
C_1 and C_2 each supports E/2	L_1 and L_2 each conducts $I_s/2$
Transformer excited by ±E/2	Transformer excited by $\pm I_s/2$
At least one switch is open	At least one switch is closed
Current stiff inductive filter	Voltage stiff capacitive filter
Suited to higher input voltages	Suited to higher input currents
Buck-derived converter	Boost-derived converter

Table 3.1 Dual Properties

In the practical implementation of the half bridge dual converter, the input current source is usually replaced with a voltage source, because two inductors act to make the voltage source current stiff. This arrangement eases the difficulties in finding a proper current source for the converter. Figures 3.3(a) and (b) respectively show the practical form of the half bridge dual converter and its waveforms. In the discussion below, the output capacitor C_o is assumed to be large enough and ripples in the output voltage are negligible.

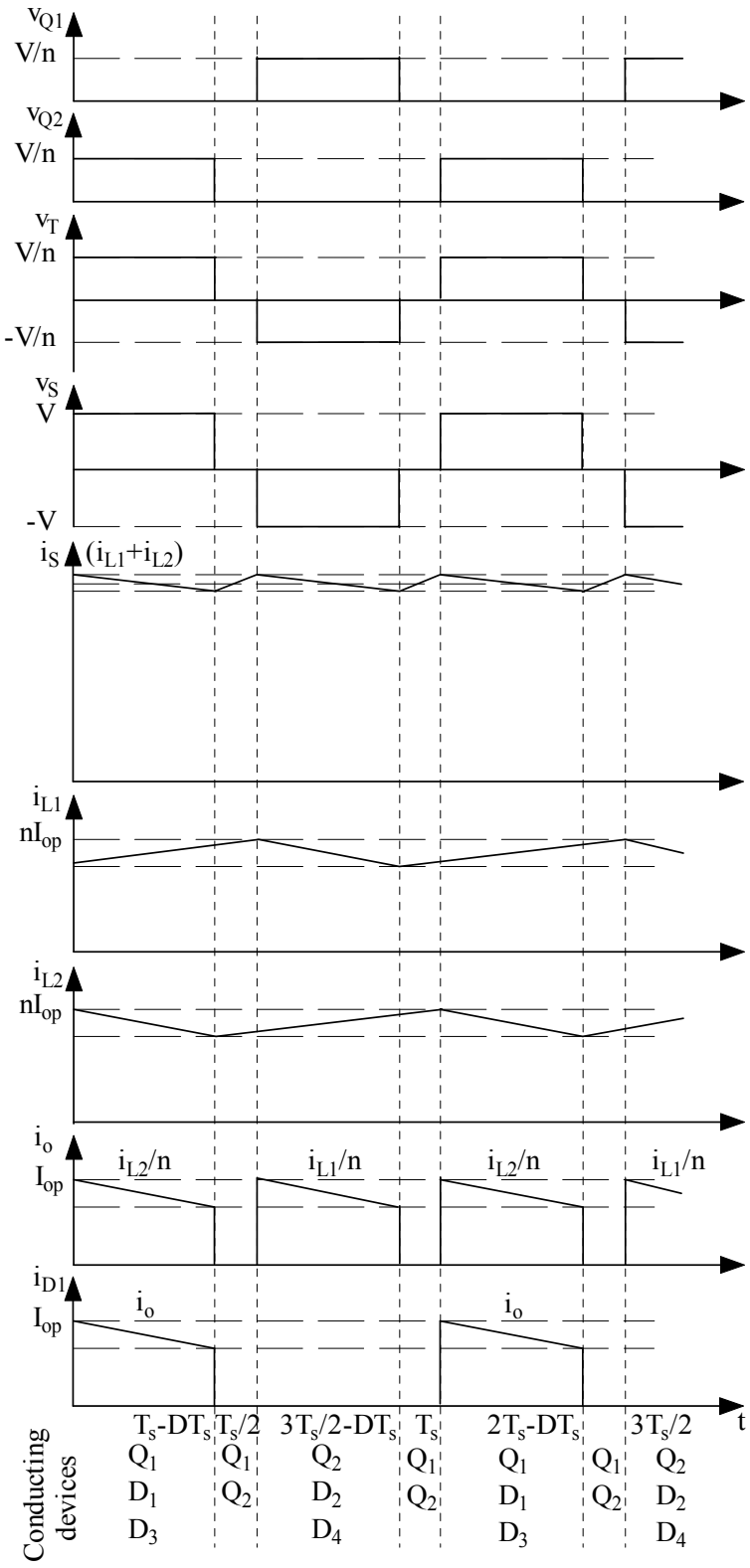
The operation of the half bridge dual converter can be divided into three stages. When Q_1 is closed and Q_2 is open, the current flowing in L_2 flows into the transformer, out of the primary winding dot and then through Q_1. When Q_2 is closed and Q_1 is open, the current flowing in L_1 flows into the transformer primary winding, dot positive, and then through Q_2. During these two stages, the power is transferred from the input source to the output load and the converter is said to be in the powering stage. When both of the switches are closed, no current flows into the transformer primary and the converter is said to be in the boost stage.

Because the half bridge dual converter is boost derived, the explanations of the basic boost converters in Appendix 1 can be readily applied here. Including the effect of the transformer, the output voltage can be calculated to be



(a)

Figure 3.3 Practical Half Bridge Dual Converter (a) Schematic



(b)

Figure 3.3 Practical Half Bridge Dual Converter (Continued) (b) Waveforms

$$V = n \cdot \frac{1}{1-D} \cdot E \tag{3.2}$$

where n is the transformer turns ratio and D is the duty cycle of each switch.

If V_d is defined as the voltage of the output capacitor referred to the transformer primary, where $V_d = V/n$, the diagram of the switch duty cycle D against the ratio of V_d/E can be drawn in Figure 3.4. The maximum allowable input voltage E must be less than one half of V_d in order to maintain the switch duty cycle to be greater than 0.5. In the half bridge dual converter, the peak switch voltage is fixed at V_d and the peak switch current equals to the supply current.

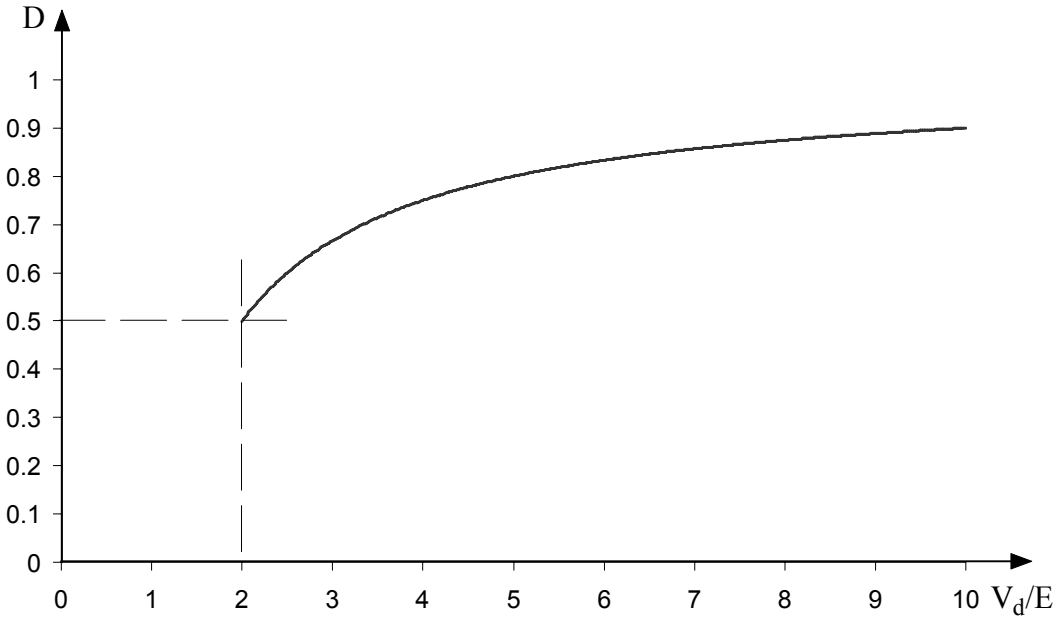


Figure 3.4 Switch Duty Cycle against the Ratio of the Voltage of the Output Capacitor Referred to the Transformer Primary and the Input Voltage

In Chapter two, the disadvantages due to higher device stresses were given for the push-pull converter operating with the input voltages ranging from $0.5\hat{E}$ to $\hat{E}$. However, in the half bridge dual converter, if a wide range of input voltages exists, the usual method is increasing the switch duty cycle instead of increasing the transformer turns ratio, which will result in higher device stresses. For example, if 51% duty cycle is used for the input voltage of $\hat{E}$, increasing the duty cycle to 75.5% can help in obtaining the same output voltage level with the input voltage of $0.5\hat{E}$ according to Equation 3.2. The turns ratio n stays unchanged and this will not cause any increase in the device voltage stresses. Waveforms under different input voltages of $0.5\hat{E}$ and $\hat{E}$ are shown in Figure 3.5.

In Figure 3.5, D' = (1+D)/2. Figure 3.5 shows that in the half bridge dual converter, the peak switch voltage is controlled by the desired output voltage and typically much less than that in a push-pull converter with the same output voltage level. Additionally, the peak diode reverse voltage does not become more adverse when operating in a wide range of input voltages. Several important device stresses for the above example with the input voltage ranging from $0.5\hat{E}$ to $\hat{E}$, are compared in Table 3.2 for the waveforms shown in Figures 2.7 and 3.5, where n is the normal transformer turns ratio.

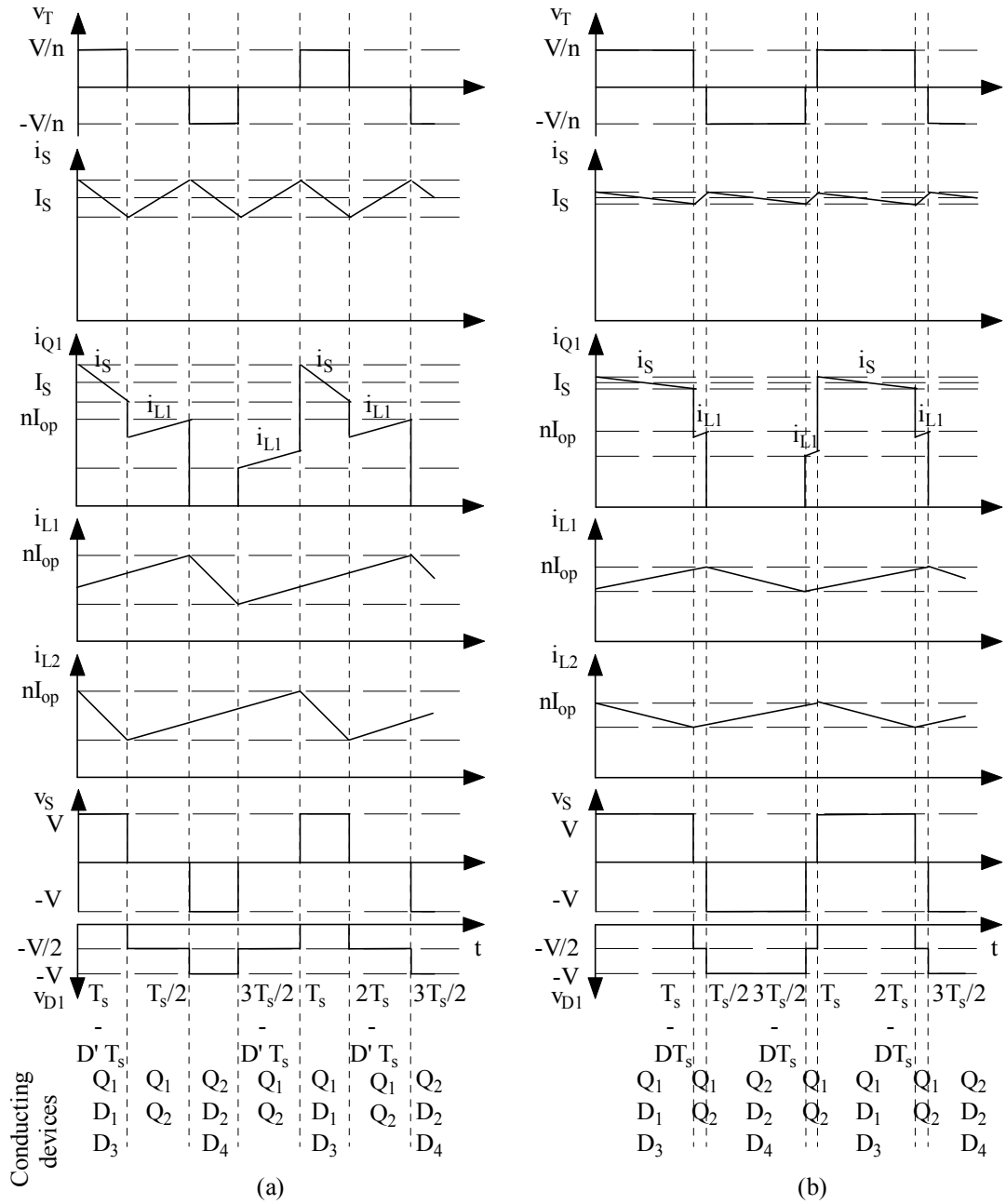


Figure 3.5 Waveforms under Different Input Voltages (a) E = 0.5 $\hat{E}$ (b) E = $\hat{E}$

The overwhelming advantages of the half bridge dual converter over the push-pull converter can be concluded as the following:

- The transformer is less prone to saturate, because it is excited by a current source.
- The copper utilization of the transformer is more efficient, because the complete primary winding is excited each time.
- The secondary side diodes do not have as severe reverse recovery problems, because a capacitive filter is used. The reverse voltage of the diodes is clamped at the capacitor voltage. Because the rectifier is current fed, the diode and transformer winding capacitance limits the rate of rise of reverse voltage, reducing recovery losses.

Item	Push-Pull Converter	Half Bridge Dual Converter
Peak Switch Voltage	$2\hat{E}$ (decided by input voltage)	V/n (decided by output voltage)
Peak Switch Current	2nI (decided by output current)	I_S (decided by input current)
Peak Diode Reverse Voltage	> 2V (decided by output voltage)	V (decided by output voltage)

Table 3.2 Comparisons of the Device Stresses

From the discussions above, conclusions can be made that both of the push-pull converter and the half bridge dual converter are suitable for PV applications, where the input voltages tend to be low, but the half bridge dual converter is a better candidate. Table 3.3 compares some main characteristics of the two converters.

Item	Push-Pull Converter	Half Bridge Dual Converter
Converter Type	Buck-derived	Boost-derived
Switch Operation	At least one switch is open	At least one switch is closed
Peak Switch Voltage	2E	V/n
Peak Switch Current	nI	I_s
Transformer Excitation	Voltage fed	Current fed
Transformer Copper Utilization	Not efficient	Efficient
Diode Reverse Recovery Problem	Exists	Does not exist
Diode Reverse Voltage	> 2V	V
Filter Type	Current stiff inductive filter	Voltage stiff capacitive filter

Table 3.3 Comparisons of the Main Characteristics

3.3 Possible Improvements

In the DC-DC converter design, size and efficiency are of prime significance. One way to reduce the size of the DC-DC converter is to increase the switching frequency. Increasing the switching frequency has at least two advantages. One advantage is to reduce the acoustic noise of the DC-DC converter in operation by increasing the switching frequency to above the upper audible frequency, which is 20kHz. The other important advantage is to make the DC-DC converter more compact or achieve a higher power packing density. In the DC-DC converter, the

magnetic components and the electrolytic capacitors are the main factors in deciding the size. These components in the DC-DC converter must be selected according to the principle that the energy stored is greater than the energy exchanged between the input source and the output load within one switching period. For a given level of power rating, the shorter the switching period, the less the energy stored. Therefore, the higher the operation frequency, the smaller the converter.

However, it does not mean that increasing switching frequencies of the DC-DC converter can reduce the size of the converter at no other costs. Increasing switching frequencies may severely reduce the total efficiency of the converter if no other measures are taken. In the DC-DC converter, the conduction and switching losses associated with the switching semiconductors are an important part of the total losses of the converter. Appendix 2 explains that the conduction loss is proportional to the semiconductor forward resistance and the switching loss is proportional to the switching frequency. An increased frequency means a higher switching loss. Moreover, unless corrective actions are taken, power losses in the magnetic components in the converter such as transformers and inductors will become greater if switching frequencies are increased. The increased loss can be explained by more significant magnetic losses in the core material or conductor eddy current effects, which generate more skin effect loss and proximity effect loss, in the winding conductors under higher frequency currents. Additionally, in the practical operation of the DC-DC converter, power losses associated with the parasitic components may also increase with the increase of the switching frequencies. Therefore, higher switching frequencies can mean higher power losses or lower efficiencies in the DC-

DC converter. In order to maintain or enhance the converter performance in higher frequencies, improvements have to be made to reduce the power losses in the magnetic components, the switching semiconductors and the parasitic components.

To reduce the conductor loss in the magnetic components, improved winding designs have to be used to alleviate the eddy current effects. One possible method is to use Litz wire technology in the windings of the magnetic components to replace the conventional solid conductors. By twisting or braiding a bunch of individually insulated wires in a uniform manner, Litz wires can appreciably increase the conductor cross section area for high frequency current flow and thus effectively counteract the skin effect. Because finer wires are more favorable to low proximity effect loss, this loss can be neglected, if the diameter of each strand in Litz wires is carefully selected. On the other hand, the skin effect loss may even be ignored, if the strands in Litz wires are very well transposed during the manufacturing, [27]. However, limitations on the number of strands do exist because dc resistance increases as the number of strands increases and this will eventually offset the reduction in eddy current loss, [28]. Magnetic core losses can be controlled by the choice of materials or reducing magnetic flux densities according to the Steinmetz empirical equation, [29].

To reduce the power loss in the switching semiconductors, two possible methods may be utilized:

- soft switching technique, and
- lossless snubbers.

Soft switching technique has been known for decades. It can make better use of the parasitic elements in the converter. By turning on and off the switches at zero current and/or zero voltage, resonant converters have ideally zero switching loss, [30]. This technique is also an indispensable technique for very high frequency DC-DC converters. However, the ratings of the switching device may significantly increase, [31], if sinusoidal voltage and current waveforms exist in the switch. The resonant converter also needs a complex control circuit to generate appropriate timings for turn on or turn off driving signals. Moreover, it is usually difficult to maintain the resonance conditions across a wide load range for resonant converters.

The snubber network is an additional circuit to the basic DC-DC converter. The major function of the snubber circuit is to reduce the electrical stresses placed on the switching semiconductors during switching transients and keep the switching semiconductors operating within the Safe Operating Area (SOA). From the energy usage perspective, snubbers can be divided into two types: dissipative snubbers and nondissipative or lossless snubbers. As explained in Appendix 3, the dissipative snubbers are capable of reducing the stresses on switches during turn on or turn off by storing the extra energy in their own networks. They usually have the simplest structures and hence the lowest costs. However, the dissipative snubbers will finally convert the stored energy into heat, usually through a resistor, in later cycles and the efficiency cannot be considerably improved, [32]. Because this power loss is

proportional to the switching frequency, [33], dissipative snubbers become more unfavorable when higher switching frequencies are required. Lossless snubbers are capable of returning the stored energy back to either the input source or the output load and are suitable for the converter design in high switching frequencies, [34]. Some designs of lossless snubbers even return the energy stored in the snubber elements to the converter control module to minimize the need for external connections, [35]. Lossless snubbers may be a good choice in reducing the power loss in the switches for the half bridge dual converter in that they can recover the energy stored in the transformer leakage inductance and stop it from being dissipated in switches, [24].

In the practical operation of the DC-DC converter, parasitic components exist because devices used cannot be deemed as ideal components. Possible parasitic components may include transformer leakage inductance, transformer primary secondary capacitance, transformer winding capacitance, output capacitance of the switching semiconductors and diode junction capacitance. Most of these parasitic components will cause extra power loss in the converter. To reduce this part of power loss, parasitic components will have to be either actively used or suppressed. As discussed above, soft switching technique could make active use of some parasitic components in the converter. Feasible ways to reduce the value of parasitic components such as the transformer leakage inductance are improved transformer construction techniques such as bifilar or coaxial winding design, [36]-[38]. By reducing the leakage inductance, the energy stored in the leakage inductance and dissipated in the switching semiconductors during turn-off is reduced. The only

challenge is to ensure that considerably more work will not be involved in the transformer fabrication compared with the traditional transformer manufacturing.

Many of these principles will be illustrated in the next two chapters. These describe variations of the converter that have been developed to illustrate the potential of the converter for MIC applications.

4. THE HARD-SWITCHED HALF BRIDGE DUAL CONVERTER

This chapter will focus on the hard-switched versions of the half bridge dual converter. To illustrate the principles of the half bridge dual DC-DC converter design, a converter will be developed for an existing solar module which consists of 44 "Saturn" cells from BP Solar. This solar module has a nominal 17.6V 88W rating. The target output voltage of the half bridge dual converter will be in the range from 340Vdc to 360Vdc, which is suitable for direct inversion to 240Vac.

4.1 A Prototype Converter

In order to provide a starting point, a prototype half bridge dual converter with 100kHz operation frequency was designed and constructed. The power losses in the key components were identified and one possible improvement was discussed.

4.1.1 Design Process

According to Figure 3.3(a), the key components in the half bridge dual converter are Inductors L_1 and L_2, Transformer T, Mosfets Q_1 and Q_2, Diodes D_1 to D_4 and Capacitor C_o. These components can be selected according to their electrical or magnetic specifications. The detailed design process is explained in Appendix 4. The components used in the circuit are:

- Inductors L_1 and L_2 – Core type Siemens RM14, ferrite grade Siemens N41, total air gap = 1.0mm, number of turns = 27, wire diameter 1.00mm (1.06mm overall).
- Transformer T – Core type Philips EC41, ferrite grade Philips 3C80, primary number of turns = 21, secondary number of turns = 212, primary wire diameter 1.00mm (1.06mm overall), secondary wire diameter 0.32mm (0.36mm overall).
- Mosfets Q_1 and Q_2 – International Rectifier IRFZ40, V_{DS} = 50V, I_D = 35A, $R_{DS(on)}$ = 0.028Ω.
- Diodes D_1 to D_4 – Philips BYT79-400, V_{RRM} = 400V, I_F = 14A, V_F = 1.05V, t_{rr} = 60ns.
- Capacitor C_o – Philips MKP capacitor 1μF.

4.1.2 Simulation Results

As the first step, simulation was performed with SIMULINK package in MATLAB program. The SIMULINK file is held on the attached CD and located in the directory of 'simulink files'. The circuit schematic for the simulation purpose is based on the idealized version of the half bridge dual converter shown in Figure 3.3(a) and does not include the parasitic elements as in the practical converter. The simulation results for the mosfet Q_1 current, mosfet Q_1 voltage, transformer T primary current, transformer T primary voltage and diode D_4 voltage are shown in Figure 4.1. The duty cycle of each switch is 55%.

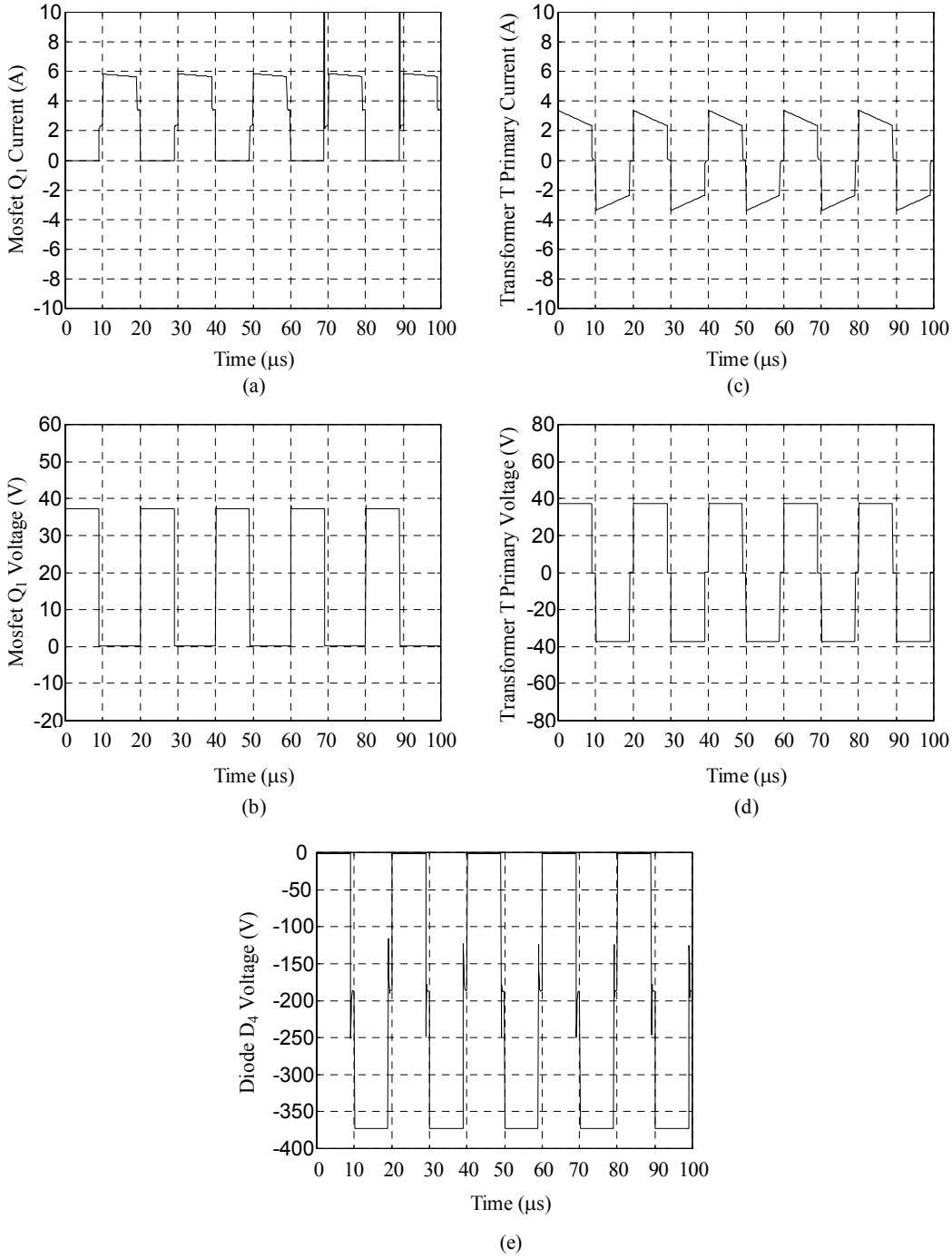


Figure 4.1 Simulation Waveforms (a) Mosfet Q_1 Current (b) Mosfet Q_1 Voltage (c) Transformer T Primary Current (d) Transformer T Primary Voltage (e) Diode D_4 Voltage

In Figure 4.1(a), the leading edges of the mosfet current sometimes show a transient current spike. This is an artefact of the simulation models used in the SIMULINK package, which can also be verified by later experimental results. The peak mosfet current, which represents the input current at that time, shows very little ripple. The ripple in the transformer primary current in Figure 4.1(c) is due to the discharging of each input current dividing inductor, L_1 or L_2. The voltage waveform of the output diode D_4 shown in Figure 4.1(e) is exceptionally clean, without any evidence of the reverse recovery problem.

4.1.3 Experimental Results

In order to verify the simulation results, the converter was constructed in the laboratory. The following texts will give the experimental results in several respects.

The driving circuit generates 50kHz mosfet gate driving signals. The circuit schematic is shown in Figure 4.2.

In the driving circuit, one National Semiconductor LM3524D is used as the pulse width modulator with the oscillation frequency set to 100kHz. Two Maxim MAX4429s translate the RTL output from LM3524D to high current output to drive the mosfet gate. The circuit resistance and capacitance values are shown in Table 4.1. The oscillation components R_{DT} and C_{DT} are selected for 100kHz.

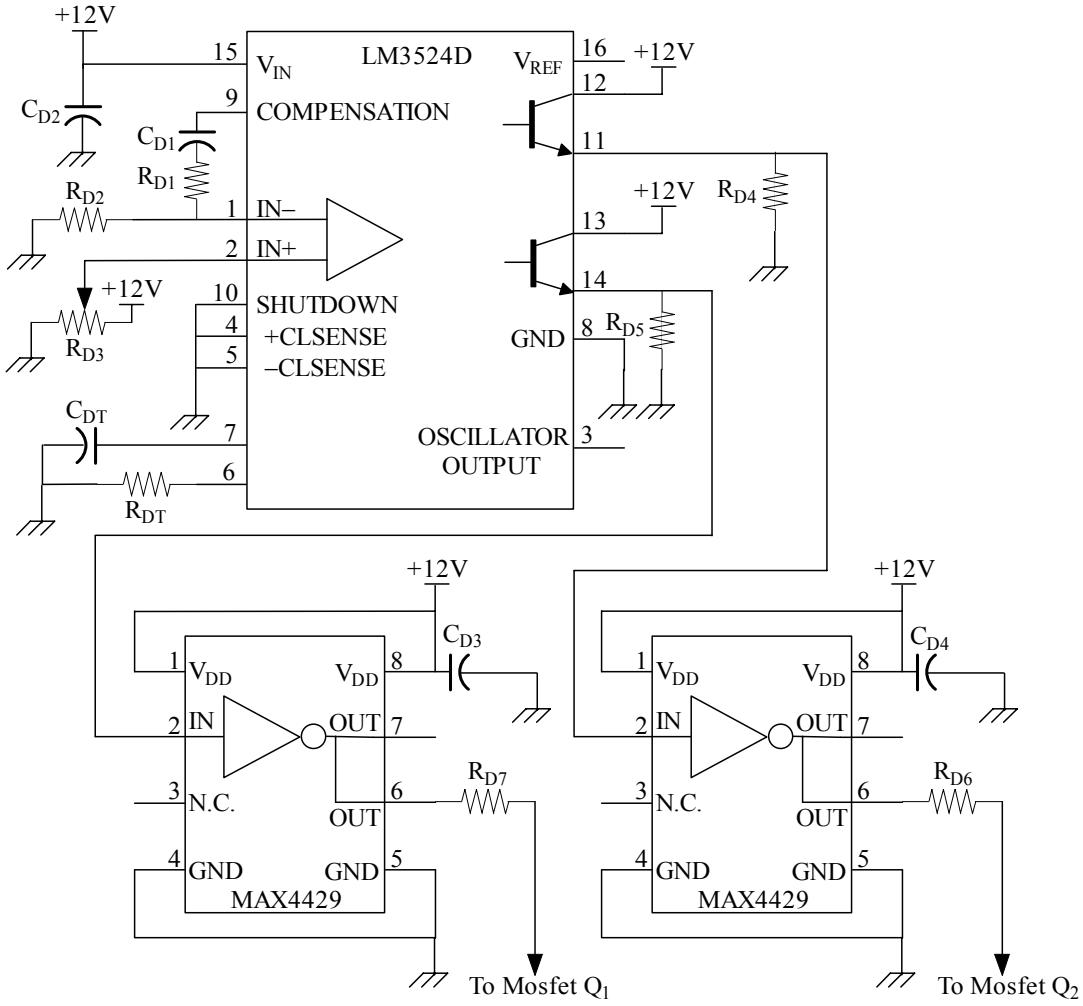


Figure 4.2 Driving Circuit

Resistor	R_{D1}	R_{D2}	R_{D3}	R_{D4}	R_{D5}	R_{D6}	R_{D7}	R_{DT}
Value	330Ω	10kΩ	20kΩ	1kΩ	1kΩ	10Ω	10Ω	2.2kΩ
Capacitor	C_{D1}	C_{D2}	C_{D3}	C_{D4}	C_{DT}			
Value	0.1μF	0.1μF	100μF	100μF	4.7nF			

Table 4.1 Resistors and Capacitors in the Driving Circuit

In the practical operation of the prototype converter, circuit inductances cause higher mosfet turn off voltages, that exceed the mosfet voltage rating. To control the over

voltage across the mosfet drain and source within the mosfet voltage rating, a relatively easy solution is to add a voltage limiting snubber at the converter primary side. Figure 4.3 shows the actual experimental circuit with the voltage limiting snubber.

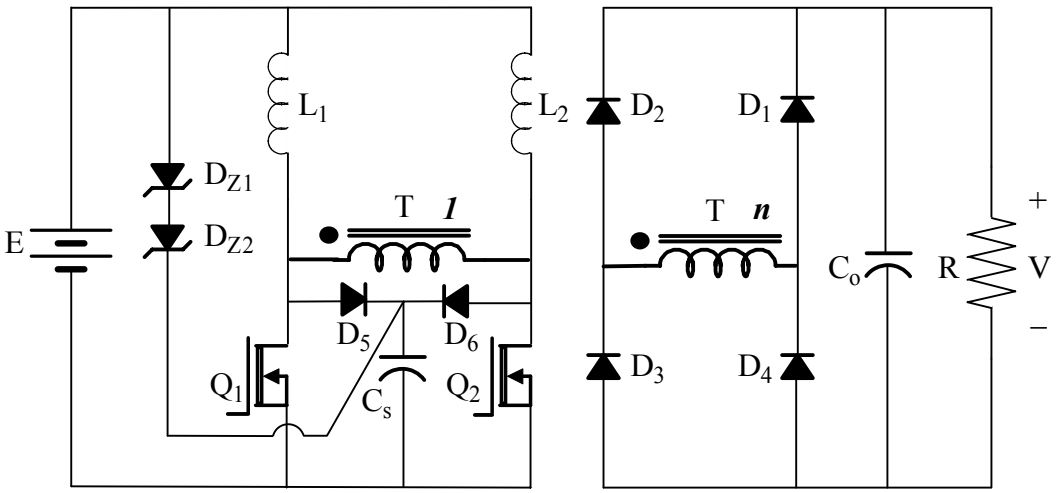


Figure 4.3 Experimental Circuit

The voltage limiting snubber is made up of two zener diodes, two Schottky diodes and one capacitor. The components used are listed below.

- Zener diodes D_{Z1} and D_{Z2} – Motorola 1N4740A, $V_Z = 10V$.
- Diodes D_5 and D_6 – SR106, $V_{RRM} = 60V$, $I_F = 1.0A$, $V_F = 0.7V$.
- Capacitor C_s – $0.1\mu F$.

Because the clamping voltage of one zener diode is 10V, two zener diodes were used in the snubber network in series to provide a clamping voltage of 20V. During the turn off of the switch, if the mosfet drain source voltage is considerably higher

than (E+20)V, two Schottky diodes, D_5 and D_6, will conduct. Current flows through the zener diodes and back to the voltage source and the energy stored in the transformer leakage inductance will be transferred partly to the voltage source instead of dissipating completely in the transformer T and the mosfets Q_1 and Q_2. By introducing the voltage limiting snubber to the converter, the over voltage across the mosfet can be easily controlled within the mosfet voltage rating at little extra cost. However, the trade off is that not all energy stored in the transformer leakage inductance is returned back to the source. Part of this energy is dissipated in the zener diodes. This effect will be shown later in this chapter.

The experimental waveforms are recorded by the oscilloscope Tektronix TDS220 and shown in Figure 4.4. The experimental waveforms match well with the simulation waveforms at the cycle by cycle time scale. As expected, small variations exist during turn on and turn off of each switch as the device models in the simulation do not contain parasitic elements such as mosfet and diode capacitances.

In Figure 4.4(a), mosfet current does not contain the spike artefact at the leading edge as shown in the simulation results. However, oscillatory currents exist at both of the leading and falling edges due to the resonance between the transformer leakage inductance and the mosfet output capacitance.

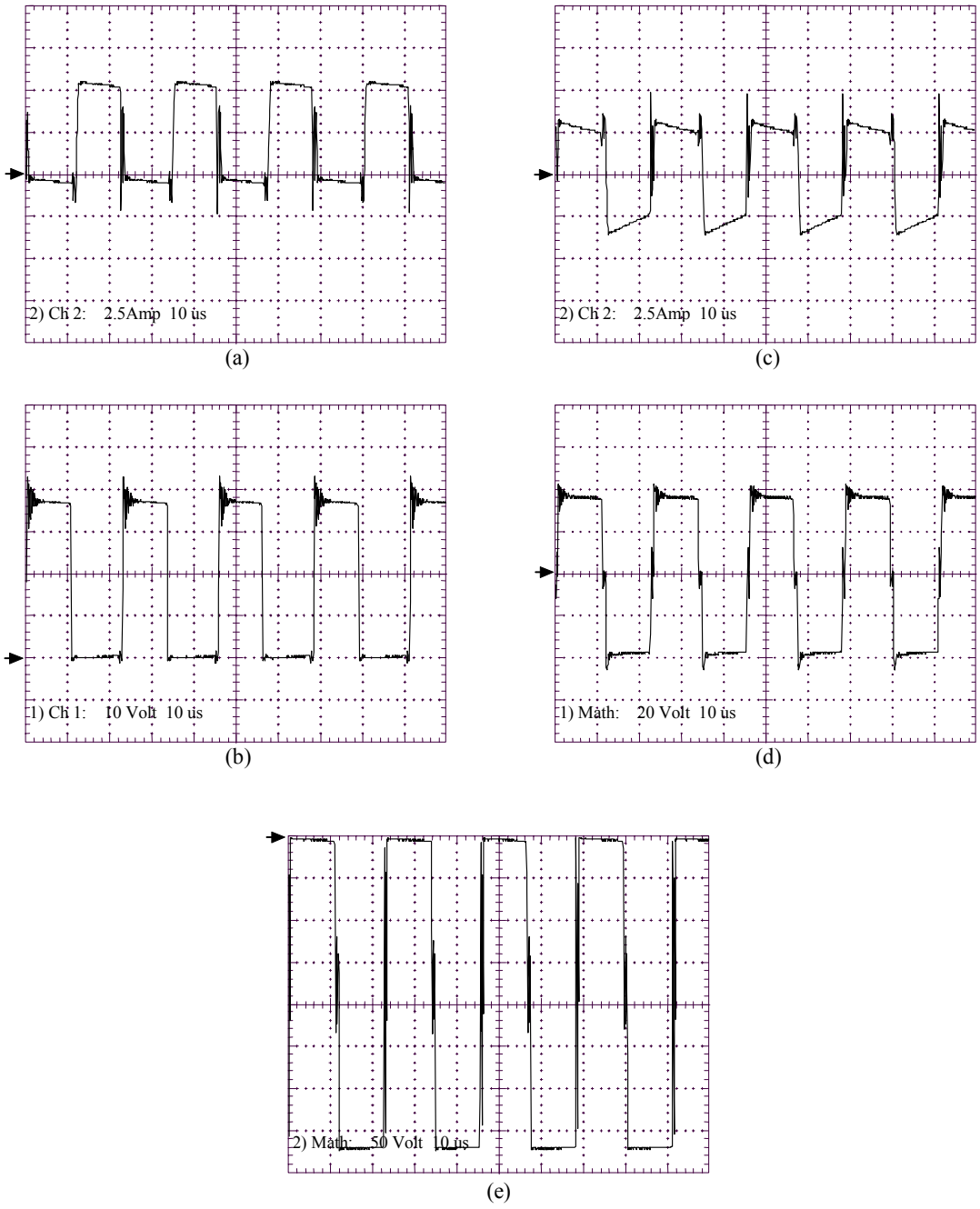


Figure 4.4 Experimental Waveforms (a) Mosfet Q_1 Current (b) Mosfet Q_1 Voltage (c) Transformer T Primary Current (d) Transformer T Primary Voltage (e) Diode D_4 Voltage

Figure 4.4(b) shows the mosfet voltage waveform. High frequency oscillation exists at the leading edge when the mosfet turns off. The first peak of this oscillating voltage can be calculated to be

$$V_{peak} = V_{off} + I_{Coss} \cdot \sqrt{\frac{L_{leakage}}{C_{oss}}} \tag{4.1}$$

where $L_{leakage}$ is the transformer primary leakage inductance, C_{oss} is the mosfet output capacitance, V_{off} is the final turn off voltage across the mosfet and I_{Coss} is the initial current injected to the capacitor C_{oss}. To lower this peak, three possible measures could be taken,

- Increasing the mosfet output capacitance,
- Reducing transformer leakage inductance, or
- Transferring the energy stored in the transformer leakage inductance to the snubber network.

Among these three methods, only the last two are feasible. Mosfet output capacitance can be increased by adding parallel capacitors but this would cause additional turn on losses. A relatively low leakage inductance, 0.7μH, is achieved by interleaving transformer primary and secondary windings, [27] and a voltage limiting snubber is introduced to the converter to transfer part of the energy stored in the leakage inductance back to the voltage source.

Of course, in this specific case, the third method is the most important in limiting the over voltage within the mosfet voltage rating. The experiment also confirmed that reducing the transformer leakage inductance by interleaving the primary and secondary windings only could not reduce the over voltage across the mosfet to a low enough level.

In the transformer primary current and voltage waveforms shown in Figures 4.4(c) and (d), the oscillation related to the transformer leakage inductance and the diode junction capacitance can be observed during the switch overlap times, when both mosfets are closed. Figure 4.4(e) confirms that the output diodes are free from any over voltages due to the reverse recovery.

As the hard-switched converter is intended to be a forerunner for higher frequency, low loss converters, significant effort was put into identifying the main sources of the power loss. The converter was operated at an input power of 86.7W. The total loss measured by the calorimetry method, [39], is 11.1W and the efficiency is 87.2%. The measurement process of the calorimetry method and the recorded data are given in Appendix 5. This measured loss is in good agreement with the total thermal loss estimation of 10.3W based on device temperature rises. Table 4.2 contains a list of the losses estimated by allowing the converter to reach the thermal equilibrium and observing temperature rises, [27]. The detailed calculation is shown in Appendix 6.

Component	Temperature Rise (K)	Estimated Power Loss (W)
Transformer T	29	3.9
Inductors L_1, L_2	18	3.2
Mosfets Q_1, Q_2	21	0.7
Zener Diodes D_{Z1} , D_{Z2}	60	2.0
Diodes D_1 to D_4	7	0.5
Total	N/A	10.3

Table 4.2 Power Loss Breakdown

The loss of 3.9W in the transformer can be reduced by better grade ferrites. Some additional transformer loss is due to oscillatory currents caused by device inductance and capacitance on both the primary and the secondary sides. The mosfet loss includes both of the conduction loss and the switching loss. Because the mosfet forward resistance of IRFZ40, 0.028Ω, is relatively low, the switching loss must be a dominant form of loss. The loss in the primary snubber, mainly in two zener diodes, could be reduced by raising the clamping voltage. However, this may result in the increased loss in both of the transformer and mosfets. Another disadvantage of raising the clamping voltage is that mosfets with higher voltage ratings are required. For the same die area, this would cause some additional conduction loss due to higher forward resistance.

4.1.4 Lossless Snubber

As stated in Chapter three, nondissipative or lossless snubbers may be a choice to recover the energy stored in the transformer leakage inductance and improve the converter efficiency. A lossless L-C resonant turn-off snubber, which is able to accomplish such a task, was first invented in 1974, [40]. Generally, passive snubbers have more advantages than active snubbers, which utilize auxiliary switches, [41], because additional switches increase the complexity of the circuit and decrease the reliability. Figure 4.5 shows a variation of the converter that includes a passive lossless snubber that is capable of recovering the energy stored in the leakage inductance and reducing the turn off switching loss, [24]. The operation will move through the following stages. Assume C_s is initially charged to –E:

- Q_1 turns off, and its drain current transfers to the loop made up of C_s, D_s and the supply E, as shown in Figure 4.6(a). The dashed line illustrates the current direction. Given the initial charge on C_s, Q_1 turns off with zero voltage.
- C_s linearly charges until the normal off state voltage is reached. Normally this is above +E.
- The stored energy in the leakage inductance continues to drive a reducing current into C_s. The current falls to zero once the leakage inductance energy is recovered. The capacitor, and the drain voltages, are driven above the normal off state voltage.

- D_s blocks in the reverse, as shown in Figure 4.6(b). The capacitor remains in this state until Q_1 conducts once more.
- At Q_1's next conduction, a resonant current is established in L_{sr}, D_{sr} and C_s, as shown in Figure 4.6(c). This current reverses the voltage polarity of C_s. Once a voltage of –E is reached, D_s conducts and allows L_{sr} to discharge into the input source E, as shown in Figure 4.6(d).

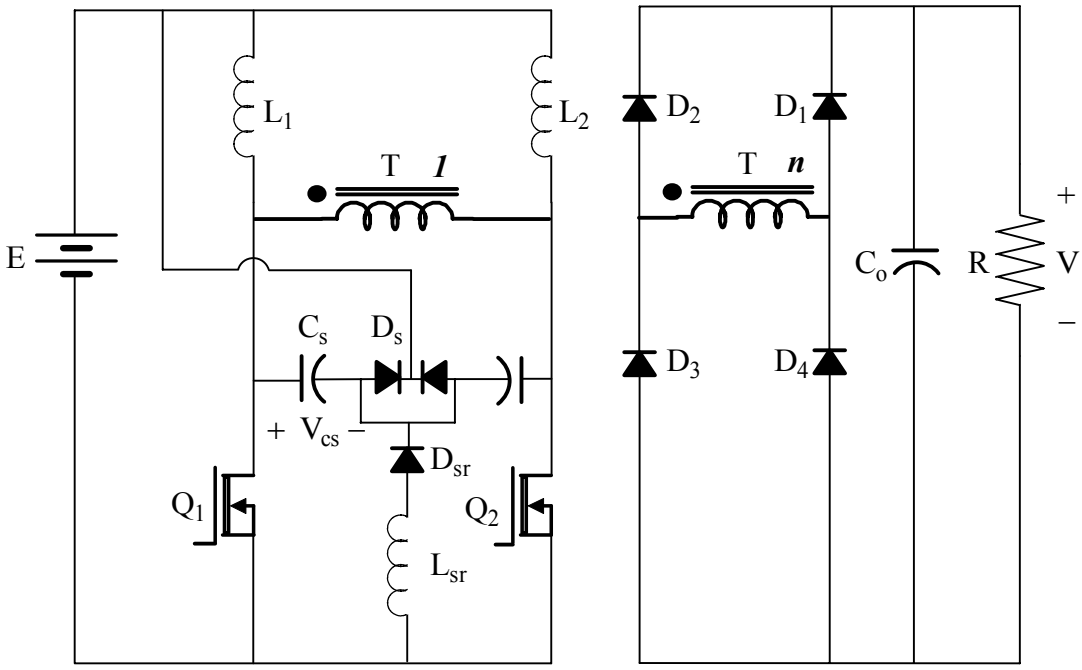


Figure 4.5 Converter with Lossless Snubber

While this approach is theoretically lossless it has some disadvantages that need attention. The circuit is relatively complex and additional components are required. Moreover, it can be practically difficult to construct the loop Q_1, C_s, D_s and the supply E. This loop needs to have very low inductance if adequate voltage clamping is to be maintained. Like many existing energy recovery snubbers, minimizing the

stray inductance could be a very challenging work, [42]. Considering the above two drawbacks of the lossless snubber design, it is not implemented and other variations are explored to achieve the half bridge dual converter of higher frequencies and higher efficiencies.

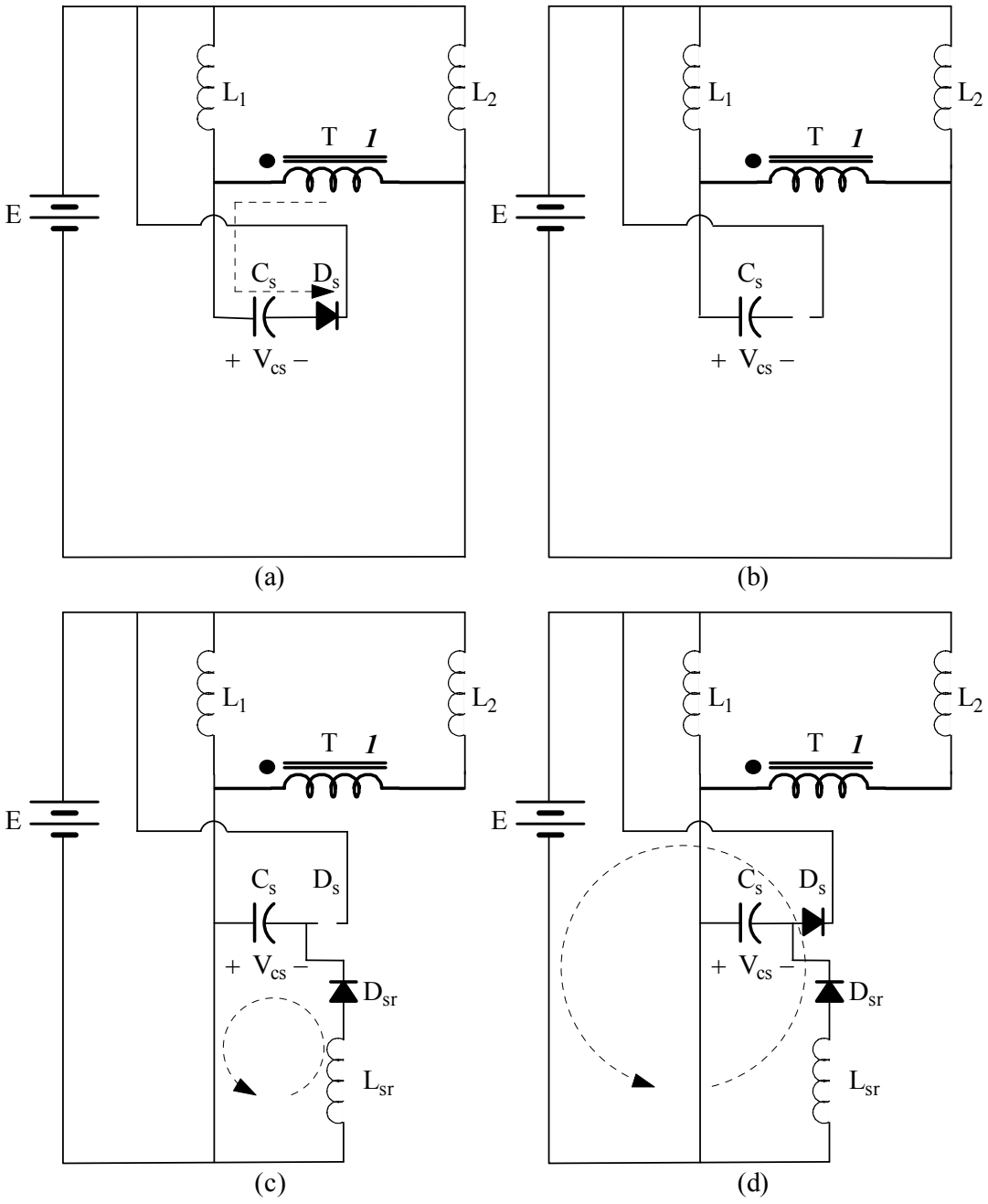


Figure 4.6 Equivalent Circuits in Analyzing Q_1's Turn-On and Turn-Off

4.2 The Half Bridge Dual Converter with a Coaxial Matrix Transformer

In the operation of the prototype half bridge dual converter, there is considerable power loss related to the leakage inductance of the transformer. Although the leakage inductance is as low as 0.7μH, referred to the transformer primary, the dissipation of the energy stored in the leakage inductance causes a high over voltage across the mosfet drain and source. A voltage limiting snubber has to be added to control this over voltage within the mosfet voltage rating. However, the energy stored in the transformer leakage inductance is not fully recovered and dissipates mainly in the voltage limiting snubber. Therefore, the dissipative snubber design is not of great benefit to improving the converter efficiency. Then it may be logical to introduce a non-dissipative snubber to the hard-switched converter but problems still exist with the implementation of the complex circuit. The issue in regard to the transformer leakage inductance presents an important barrier to raising the switching frequencies. The following sections will introduce a new hard-switched converter utilizing multiple transformers with coaxial windings to overcome the problems related to the transformer leakage inductance. This converter is of the same input voltage and power rating, 17.6V and 88W. The target output voltage is 340V. The operation frequency is 250kHz, 250% higher than that of the prototype converter.

4.2.1 Topology

Multiple transformers can be connected in matrix arrangements to achieve higher effective turns ratios, [43]. A high step up ratio is gained by paralleling transformer

primaries and series connecting secondaries. Most often, the matrix approach is used to connect many low profile transformers together to achieve high ratings in very low profile power supplies. The transformers are often based on printed circuit windings.

Coaxial winding transformers offer low leakage inductance characteristics, [36]-[38]. Since it is easy to construct coaxial winding transformers with 1:1 turns ratio, it makes sense to use matrix connection method to secure a low inductance higher turns ratio transformer.

The above two ideas are married to give the converter shown in Figure 4.7. Five coaxial transformers with 1:1 turns ratio are used in this converter. On the input side, the transformer primaries are parallel connected. On the output side, instead of directly connecting the secondary windings in series, each winding is applied to a capacitive output voltage doubler, [44]. The rectifier outputs are then series connected. As discussed later this gives two advantages, the application of Schottky rectifiers and a reduction in wiring inductance. It is expected that a very low effective leakage inductance can be achieved by this design due to the following two features:

- Low leakage inductance of the coaxial winding transformers, and
- Paralleling five transformer primaries.

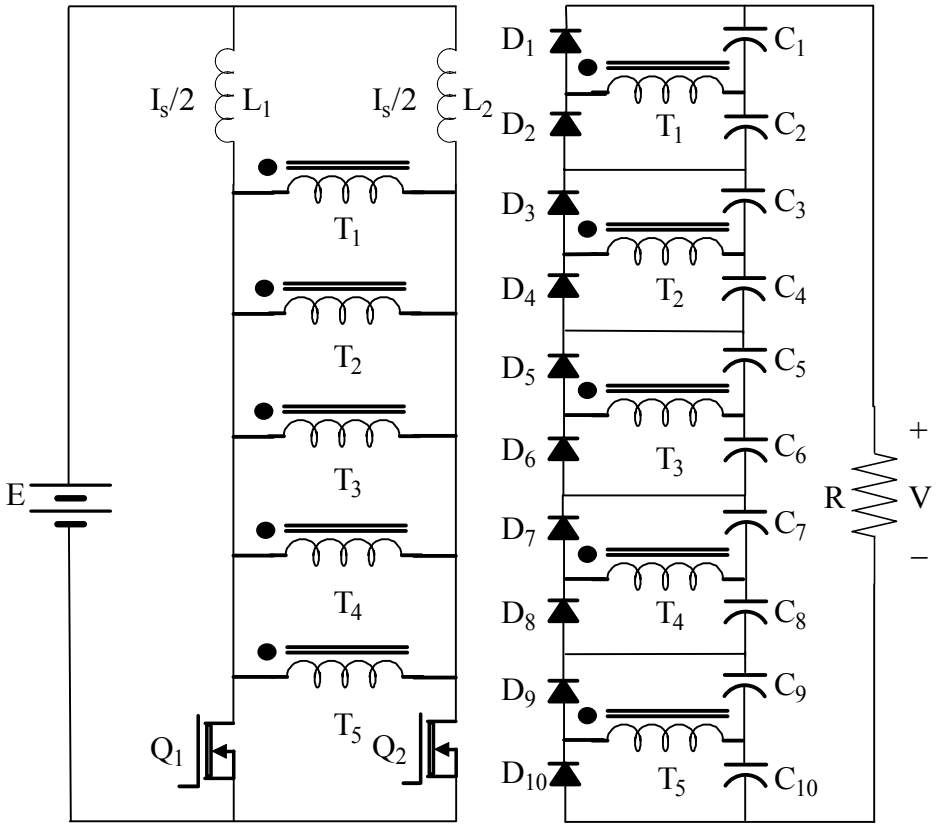


Figure 4.7 The Half Bridge Converter with a Coaxial Matrix Transformer

Considering the voltage doubling property in the converter secondary, the output voltage given in Equation 3.2 must be adjusted to be

$$V = 2 \cdot n \cdot \frac{1}{1-D} \cdot E \tag{4.2}$$

where n is the effective turns ratio of the matrix transformer and equals to 5 in this specific topology arrangement. By substituting an extreme D value of 50% into Equation 4.2, an output input voltage ratio of 20 can be obtained. This ratio is roughly the same as 340Vdc output divided by 17.6Vdc input. Of course, the output

input voltage ratio in the practical converter should be slightly higher than 20 since D values have to be greater than 50%.

4.2.2 Coaxial Winding Technique

Coaxial winding transformers, which are more commonly used in the radio frequency range, have been successfully used in many DC-DC converters, [36]-[38]. Because of their unique leakage flux distribution, which is confined within the inter-winding area, coaxial transformers have advantages in providing low core and copper loss, and low leakage inductance, [36]. The leakage inductance of the coaxial transformer depends on the winding conductor length. The leakage inductance per unit length, in Henry per meter (H/m), is

$$L_{coaxial} = \frac{N_s^2 \cdot \mu_0}{4\pi}\left[\frac{1}{2} + 2\ln\left(\frac{r_{pi}}{r_s}\right)\right] \tag{4.3}$$

where N_s is the number of secondary turns per primary turn, μ_0 is the permeability of free space, r_{pi} is the inner radius of the outer conductor, and r_s is the outer radius of the inner conductor, as shown in Figure 4.8. It is possible to construct coaxial cables with multiple central conductors, hence the unusual variable N_s is introduced.

In the experiment, Soundlink single core audio shielded cable SHW1207, [45] was used as the coaxial wire but with minor modification of replacing the original outer insulation with thinner insulation in order to fit enough turns into the transformer

core former. Some key values of the coaxial wire used in the converter are listed below.

- Number of secondary turns per primary turn $N_s = 1$,
- Inner radius of outer conductor $r_{pi} = 0.51$mm,
- Outer radius of inner conductor $r_s = 0.225$mm,
- Total winding length $l_w = 1.56$m.

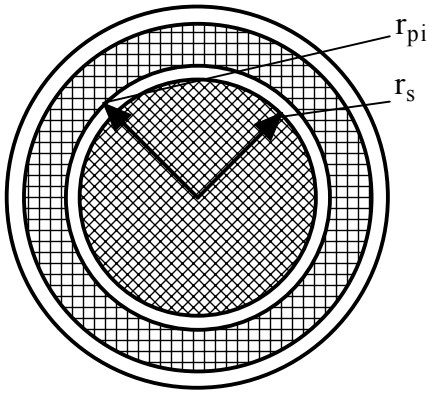


Figure 4.8 Cross Section of the Coaxial Winding

By substituting the above values to Equation 4.3 and multiplying the result by the total winding length, the leakage inductance of the transformer can be calculated as 0.333μH. Even this value is lower than the leakage inductance obtained by simply interleaving the primary and secondary windings in the prototype converter. Because the final effective leakage inductance is the parallel of the five, a significantly lower effective leakage inductance can be obtained.

During the fabrication of the coaxial winding transformers, special attention has to be paid at the termination of the coaxial winding, because primary and secondary conductors are required to be separated for mounting purposes. The end of the winding is no longer concentric and a higher leakage flux may occur. However, this effect can be negligible in the condition that the length of the termination be short enough.

4.2.3 Design Process

The design process of the key components in this converter is similar to that in the prototype converter, which is given in Appendix 4, and will not be repeated here. The components used in this converter are listed below.

- Inductors L_1 and L_2 – Core type Siemens RM14, ferrite grade Siemens N41, total air gap = 1.0mm, number of turns = 17, wire diameter 1.00mm (1.06mm overall).
- Transformers T_1 to T_5 – Core type Philips ETD34, ferrite grade Neosid F44, primary number of turns = secondary number of turns = 26, coaxial wires.
- Mosfets Q_1 and Q_2 – Siemens SDP14N05 surface mount mosfets, V_{DS} = 55V, I_D = 14.0A, $R_{DS(on)}$ = 0.1Ω.
- Diodes D_1 to D_{10} – Motorola MBRS1100T3 surface mount diodes, V_{RRM} = 100V, I_F = 1.0A, V_F = 0.75V.
- Capacitors C_1 to C_{10} – AVX surface mount capacitors, 0.47μF.

4.2.4 Simulation Results

Before constructing the converter, simulation was performed with SIMULINK. The simulation circuit schematic is based on the circuit shown in Figure 4.7. The corresponding SIMULINK file is held on the attached CD. The simulation voltage waveforms of mosfet Q_1, transformer T_1, capacitor C_{10} and diode D_{10} under the switch duty cycle of 55% are shown in Figure 4.9. In Figure 4.9(c), small ripples caused by the charging and the discharging currents are observable in the voltage waveform across the output capacitor in the voltage doubler.

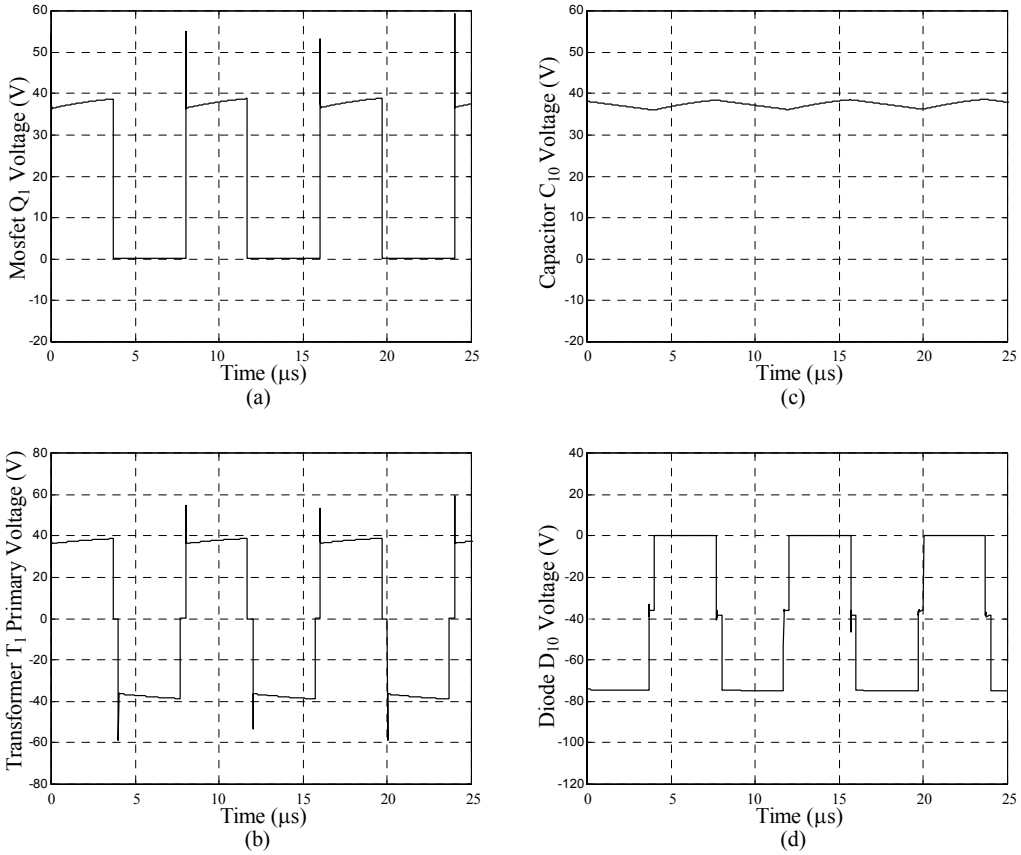


Figure 4.9 Simulation Waveforms (a) Mosfet Q_1 Voltage (b) Transformer T_1 Primary Voltage (c) Capacitor C_{10} Voltage (d) Diode D_{10} Voltage

4.2.5 Experimental Results

A photo of the experimental converter is given in Appendix 7.

The driving circuit for this hard-switched converter is the same as shown in Figure 4.2, except that the frequency of the mosfet gate driving signal is 125kHz. Accordingly, the value of the external timing capacitor has to be changed to 1.8nF with the external timing resistor staying at 2.2kΩ to set the oscillation frequency of LM3524D to 250kHz.

In the construction of this hard-switched converter care was taken to reduce any stray inductance as these contribute to undesirable voltage spikes across the mosfets. Each of the mosfets Q_1 and Q_2 in the experimental circuit was implemented as four parallel connected surface mount mosfets distributed amongst the transformers to reduce wiring inductance effects. Another advantage of this arrangement is that the reduced mosfet conduction loss can be easily achieved due to paralleling of mosfet forward resistances.

Schottky diodes, with 100V rating, could be used in the rectifier stage. The capacitive output filter used in this configuration directly clamps the diode reverse voltage and this assists in the use of low voltage rating devices. The Schottky diode forward drop, about 0.75V for these devices, is important in this case as the output load current flows through ten diodes in all. This results in a reasonable amount of conduction loss, about 2% of the converter rating.

The leakage inductance is measured by Philips programmable automatic RCL meter PM6304. The measured leakage inductance of each transformer is 425nH. This value is comparable to the calculated value of 333nH.

Figure 4.10 shows the experimental results. The waveforms are in good agreement with the simulation results except for the effects caused by parasitic elements which are not included in the simulation.

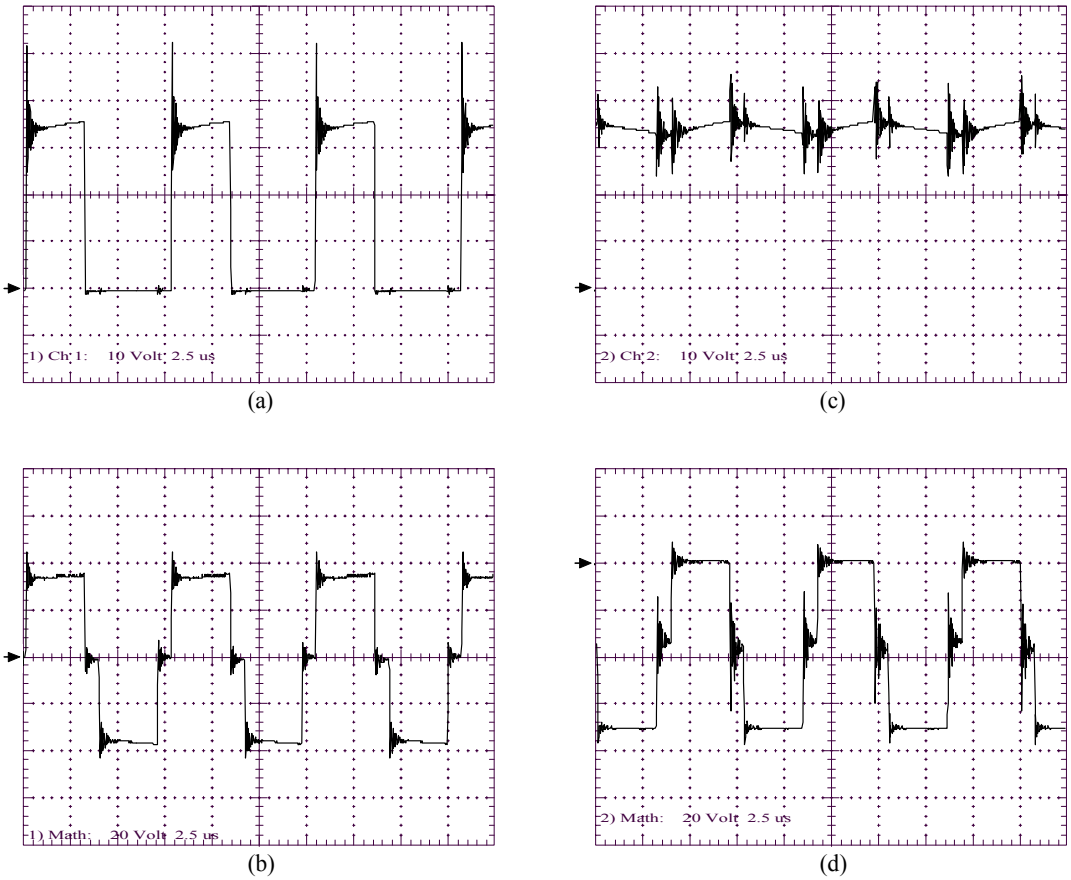


Figure 4.10 Experimental Waveforms (a) Mosfet Q_1 Voltage (b) Transformer T_1 Primary Voltage (c) Capacitor C_{10} Voltage (d) Diode D_{10} Voltage

High frequency oscillations are visible at the leading edge of the mosfet voltage waveform due to resonance between the transformer leakage inductance and the mosfet output capacitance when the mosfet turns off. As shown in Equation 4.1, this turn off peak voltage is determined by the characteristic impedance presented by the transformer leakage inductance and the mosfet output capacitance and will increase as the effective transformer leakage inductance increases. In this case, the total inductance is so low that the voltage spike is controlled within the mosfet voltage rating without the help of any other voltage clamping devices.

On the rectifier side, ripples in the voltage waveform of capacitor C_{10} in Figure 4.10(c) are small due to the high operation frequency. Same as in the prototype converter, high frequency oscillations occur when both mosfets conduct during the overlap time. Since the transformer primary voltage is clamped to zero, the parasitic capacitances of the diodes resonate with the leakage inductance of the transformer. As expected, reverse recovery cannot be seen in the diode voltage waveform shown in Figure 4.10(d).

4.2.6 Power Loss Analysis

After constructing the converter, significant effort has been made in identifying the power loss in the key components to establish possible mechanisms for further improvement.

A total power loss of 10.2W was measured by the calorimetry method. As the input power in the experiment is 89.8W, the converter efficiency is 88.6%. The recorded data are given in Appendix 5. A breakdown of the power losses estimated by temperature rise or electrical specifications of the key components in the converter is shown in Table 4.3. The estimated total loss of 10.2W matches very well with the power loss measured by the calorimetry method.

The power loss estimation of transformers and inductors were made according to their observed temperature rise and the resulting estimates of heat transfer by radiation and convection. The power loss of the mosfets and the diodes were estimated by the calculation according to their electrical specifications. The recorded temperature rise and the detailed calculation process are given in Appendix 6. From Appendix 6, we can see that, as the converter is hard-switched, a significant part of power loss in the mosfets, 2.2W, is the switching loss.

Component	Estimated Power Loss (W)
Transformers T_1 to T_5	4.0
Inductors L_1, L_2	1.3
Mosfets Q_1, Q_2	2.9
Diodes D_1 to D_{10}	2.0
Total	10.2

Table 4.3 Power Loss Breakdown

The 4W transformer loss is much higher than the design value of 0.88W. In order to further investigate this unexpected result, open circuit and short circuit experiments were performed. Figures 4.11 and 4.12 respectively show the circuit diagrams for these two experiments.

Both experiments use a linear amplifier as an excitation source. In the open circuit experiment, a variable frequency sine wave source, six operational amplifiers, a step up transformer with the turns ratio of 1:6 and a resonant capacitor are used. The operational amplifiers, National Semiconductor TL081, have to be paralleled to supply an adequate signal level at the secondary side of the step up transformer, if the transformer under test can be "power factor corrected" by the resonant capacitor. The input to the transformer under test must be of the same volt-seconds as operated in the converter in order to obtain the accurate core loss. Components used in the short circuit experiment are the same as those in the open circuit experiment, except that a step down transformer with the turns ratio of 6:1 is used to provide higher current level and the resonant capacitor is removed from the experimental circuit. These tests established the total core loss and copper loss of 0.6W and 0.5W respectively. The recorded data and calculation are given in Appendix 8.

From the total identified core loss and copper loss of the transformers, conclusion can be made that the total observed transformer loss of 4W included about 2.9W additional parasitic losses.

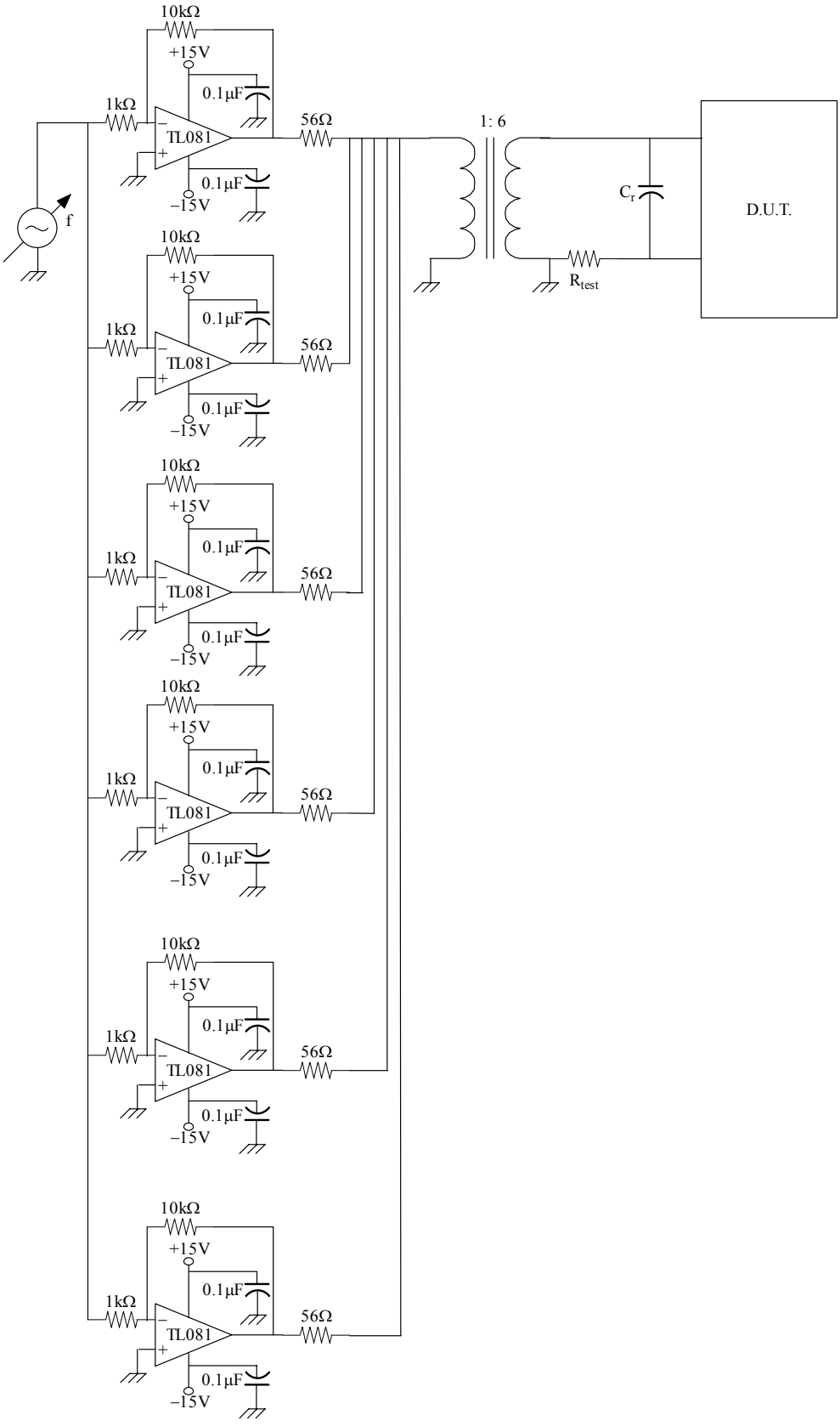


Figure 4.11 Transformer Open Circuit Experiment

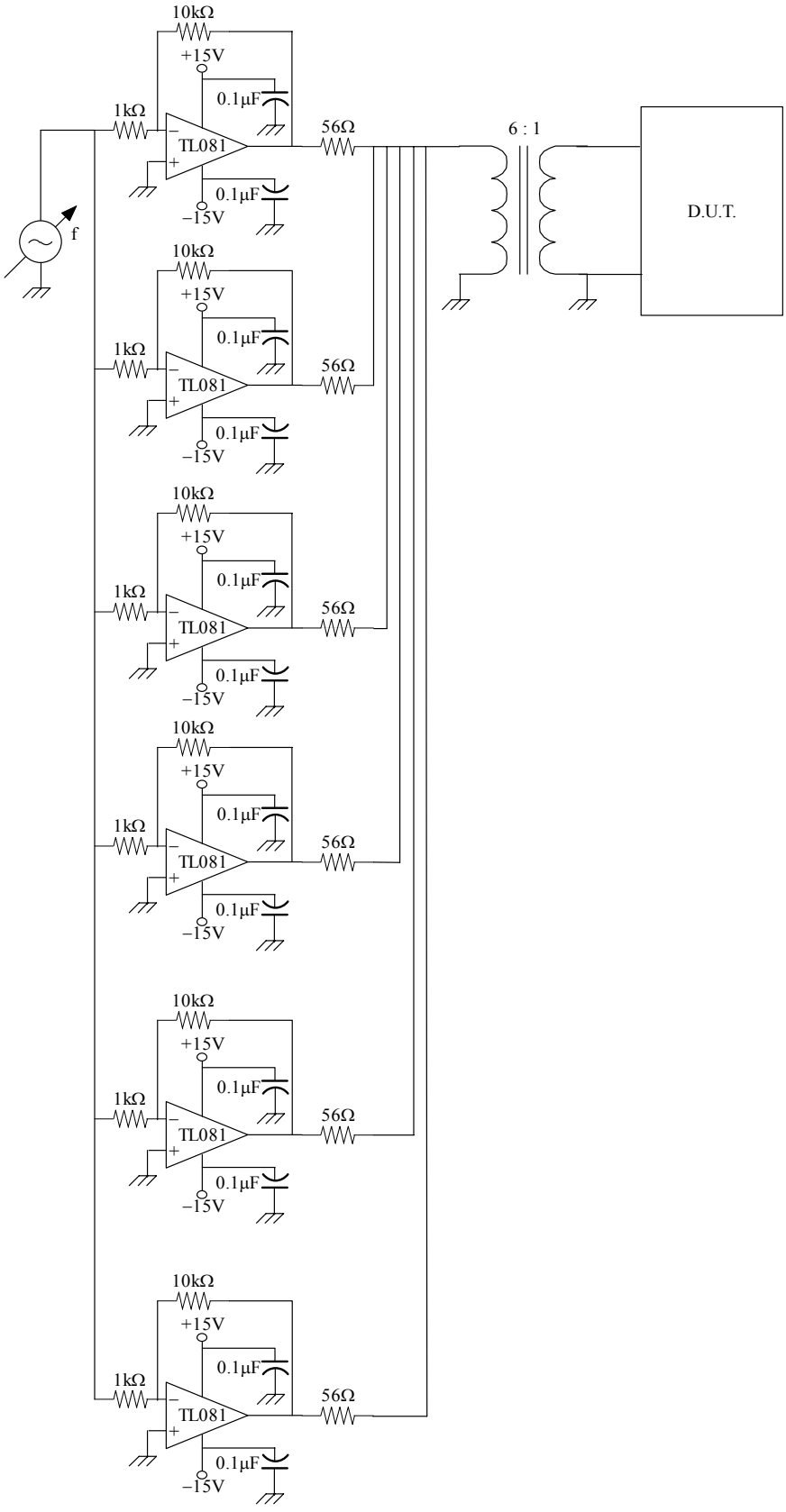


Figure 4.12 Transformer Short Circuit Experiment

Possible parasitic losses could be traced to the following sources:

- The loss related to the high frequency oscillation when the mosfets turn off,
- The loss in the resonance between the transformer leakage inductance the diode junction capacitance when both mosfets conduct, and
- The loss associated with the transformer primary secondary capacitance.

4.2.7 Possible Loss Reduction Methods

In the first two sources of parasitic losses in the transformers, oscillatory currents are usually of very high frequencies and significant skin effect exists. The oscillatory currents dissipate energy held in parasitic capacitances. For example, an output diode may be subject to the maximum reverse voltage, 340V, during a powering stage. When the converter leaves the powering stage, both primary mosfet conducts, short circuiting the transformer primary. The charged diode capacitances drive oscillations with the transformer primary leakage inductance which dissipate the capacitance energy, ending with each diode blocking around 50% of the output voltage. The energy is dissipated either in ohmic resistances – largely winding resistance due to skin effects – or in dielectric losses related to the capacitive components. The only remedy is to reduce parasitic capacitance.

Another major component of parasitic losses in the transformer, at least 1.1W, is traced to the primary-secondary capacitance. The winding capacitance is directly

measurable as the self capacitance between the inner and the outer conductors of the coaxial windings. The inter winding capacitance of each transformer is subject to voltage step changes during switching and parasitic oscillations result. This effect can be illustrated more clearly by Figure 4.13.

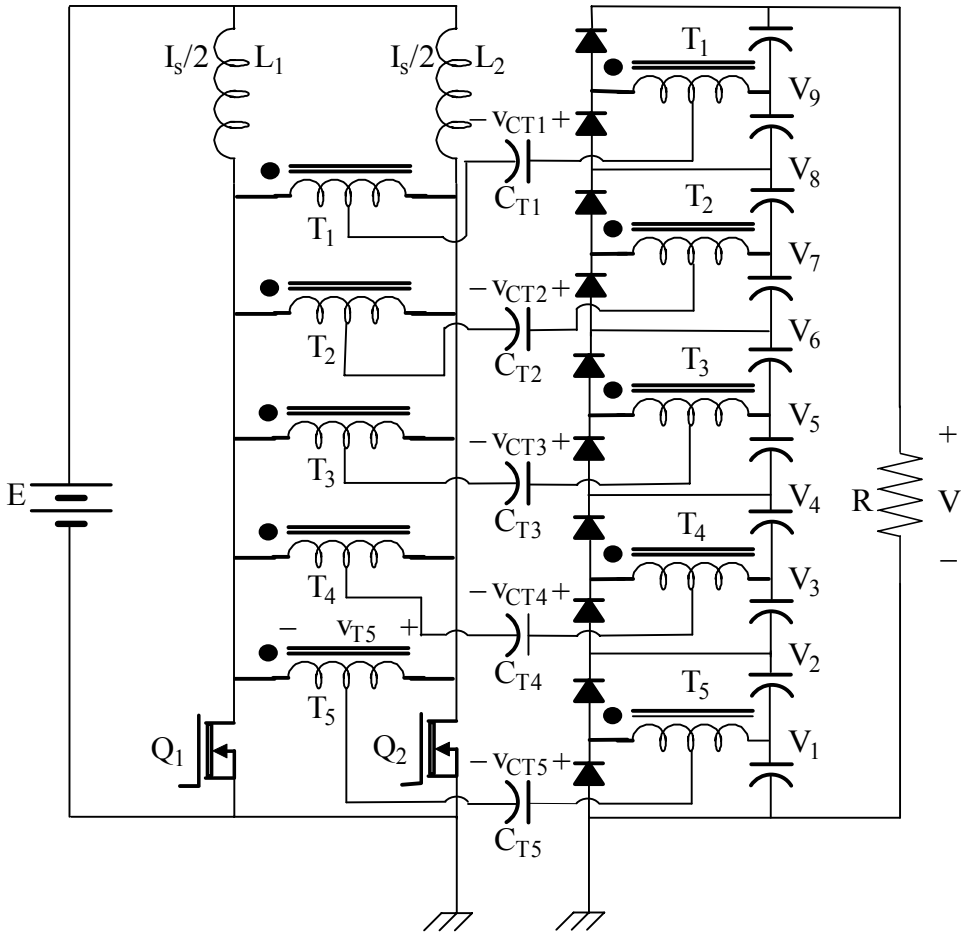


Figure 4.13 Transformer Primary-Secondary Capacitance

Assuming that the output voltage V is equally distributed across ten output capacitors, $V_1 = V/10 = \hat{V}$. The voltage across parasitic capacitance C_{T5} is initially assumed to be the difference between the mid-point voltages of the primary and the

secondary windings of the transformer T_5. The capacitor voltage v_{CT5} moves through four stages.

- Stage 1

  Q_1 is on and Q_2 is off, $v_{CT5} = \hat{V}/2 - \hat{V}/2 = 0$;

- Stage 2

  Q_1 stays on and Q_2 begins to turn on, $v_{CT5} = \hat{V} - 0 = \hat{V}$;

- Stage 3

  Q_1 begins to turn off and Q_2 stays on, $v_{CT5} = 3\hat{V}/2 - \hat{V}/2 = \hat{V}$;

- Stage 4

  Q_1 begins to turn on and Q_2 stays on, $v_{CT5} = \hat{V} - 0 = \hat{V}$.

After stage 4, same cycle repeats for C_{T5}. The voltage waveforms of the transformer T_5 primary and the capacitor C_{T5} are shown in Figure 4.14.

Therefore, in each switching period, v_{CT5} changes from $\hat{V}$ to 0. Using the same method, we know that, in each switching period, v_{CT4} changes from $3\hat{V}$ to $2\hat{V}$, v_{CT3} changes from $5\hat{V}$ to $4\hat{V}$, v_{CT2} changes from $7\hat{V}$ to $6\hat{V}$ and v_{CT1} changes from $9\hat{V}$ to $8\hat{V}$.

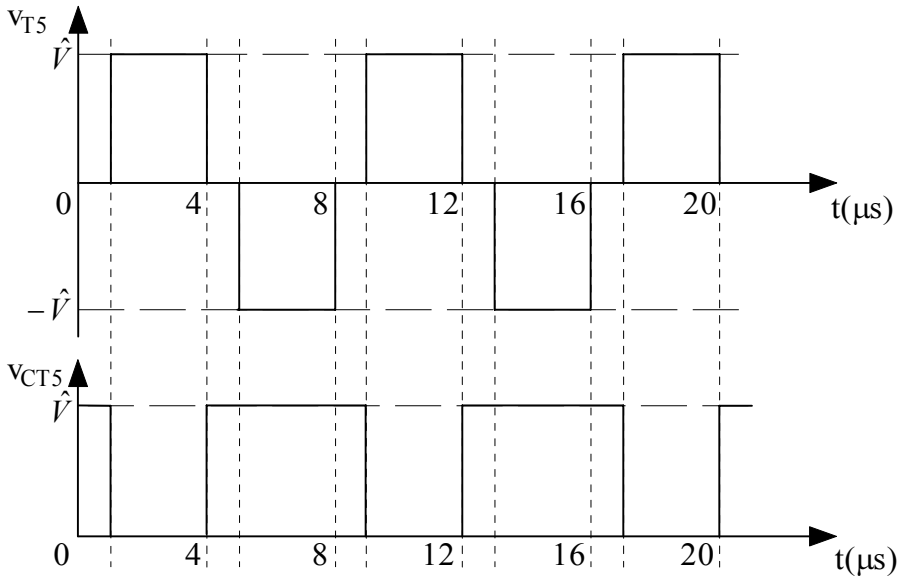


Figure 4.14 Transformer T_5 Primary and Capacitor C_{T5} Voltage Waveforms

To simplify the above analysis, the primary-secondary capacitance can also be assumed to be connected to the non-dotted end of the transformer and the voltage across the capacitance is then the difference between the changing mosfet Q_2 drain voltage and the fixed secondary capacitor voltage. Same results for the voltage change across each parasitic capacitance can then be easily obtained.

The measured capacitance between the transformer primary and secondary is 352pF. The power loss in capacitor C_{T5} is

$$P_{CT5} = \frac{1}{2} C_{T5} \hat{V}^2 f_s \tag{4.4}$$

where C_{T5} = 352pF, $\hat{V}$ = 34V, f_s =125kHz. Thus, the power loss in capacitor C_{T5} is 0.025W. If we set $\hat{P} = P_{CT5}$, then for the total of five primary-secondary capacitances, the loss would be $45\hat{P}$, since the voltage changes of $3\hat{V}$ to $2\hat{V}$, $5\hat{V}$ to $4\hat{V}$, $7\hat{V}$ to $6\hat{V}$ and $9\hat{V}$ to $8\hat{V}$ respectively lead to the power losses of $5\hat{P}$, $9\hat{P}$, $13\hat{P}$ and $17\hat{P}$. The calculation shows that the total loss related to five primary-secondary capacitances is 1.1W.

This energy stored in the primary-secondary capacitances is dissipated in the transformer copper by high frequency oscillatory currents. In most parasitic cases, the oscillation frequency is very high, and the transformer windings have significant resistances due to the skin effect.

In order to reduce the power loss in the parasitic capacitances, we can shift the ground of the secondary side to the point of V_5, i.e., $V_5 = 0$. Then the total power loss in the parasitic capacitances would be reduced to $25\hat{P}$, which is 0.6W. Figure 4.15 shows a bar chart of the loss distribution related to the primary secondary capacitance among five transformers in these two different ground arrangements. However, according to Appendix 5, the 0.5W power loss difference will only result in 0.5°C difference in temperature rise and it cannot be easily identified by the calorimetry method, because the temperature sensors used, National Semiconductor LM35s, only have a guaranteed accuracy of 0.5°C.

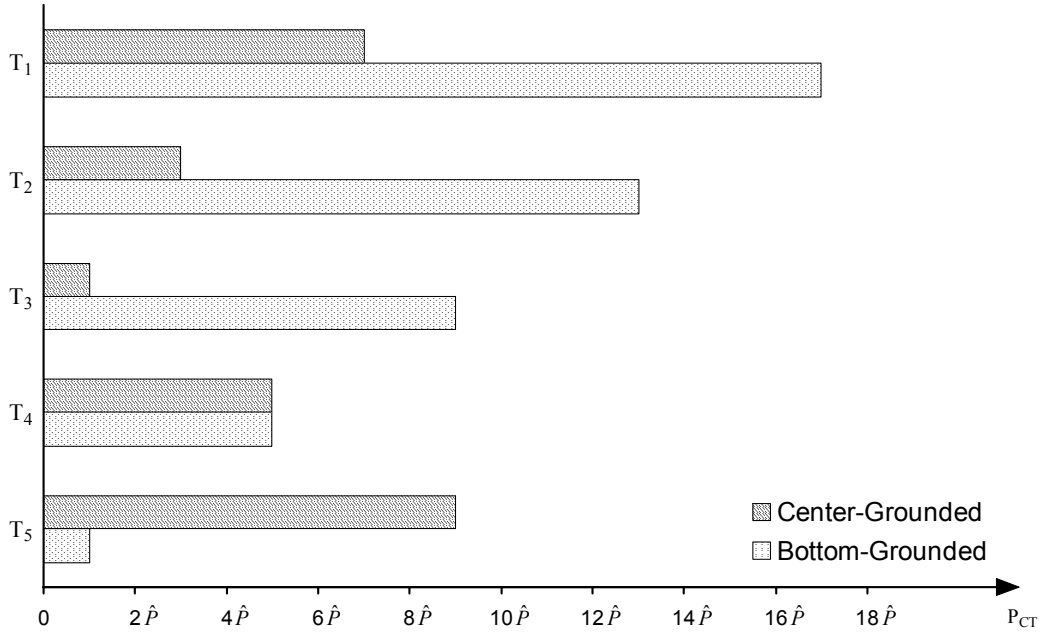


Figure 4.15 Transformer Primary Secondary Capacitance Loss Distribution

4.3 Summary

The experimental work indicates that we have reached the limit for hard-switched converters. After the construction of these two hard-switched converters, it appears that further increases in the operation frequency cannot be realized unless the converter is tolerant of the parasitic elements, especially the transformer leakage inductance, the inter-winding capacitance and the device capacitances for the primary mosfets and the output rectifier diodes. Therefore, in order to further increase the converter operation frequency and still maintain a reasonable efficiency, the only solution is to use these parasitic elements actively. Chapter five will describe resonant converters with this capability.

5. The Soft-Switched Half Bridge Dual Converter

In the previous chapter, the limitations of hard-switched versions of the half bridge dual converter were established.

Resonant or soft switching techniques have been used in high frequency DC-DC converters for more than fifty years, [46] and are marked by theoretically zero switching loss. Obviously, this characteristic is very favorable to the high frequency operation of the half bridge dual converter in that it is capable of reducing the total power loss and increasing the efficiency. The half bridge dual converter topology is sensitive to the transformer leakage inductance in the practical operation. If the resonant feature is applied to the converter, the leakage inductance will be actively utilized and is no longer an adverse factor.

This chapter will introduce the resonant form of the half bridge dual converter. The input voltage is 20Vdc and the power rating is 88W. The target output voltage is 360Vdc.

5.1 Comparisons of the Hard-Switched and the Soft-Switched Converters

According to the switching characteristics of the switches in electronic converters, there are two main approaches: the hard-switched converters and the soft-switched converters. The simplified voltage, current and power loss waveforms of the switch during the switching period for each group of converters are respectively shown in

Figures 5.1 and 5.2. Because only switching characteristics are discussed here, the corresponding waveforms during complete on and off states are omitted.

In Figure 5.1, the switch voltage and current waveforms in the hard-switched converters show overlaps of both values at high levels. Therefore, the energy dissipation during turn on or turn off period, characterised by the area below the power loss curve, is very high.

However, in soft-switched converters, the energy dissipated during turn on or turn off period is potentially zero. The switches in soft-switched converters turn on and off under zero current and/or zero voltage and ideally there is no switching loss. In the practical operation, during the transient switching period, either the current or the voltage is limited to increase at a much lower rate compared with the rates in hard-switched converters and overlaps of high voltage and current are definitely avoided, as shown in Figure 5.2. Therefore, the energy dissipation exists but is much smaller and could usually be ignored if the rate of the current or voltage increase is low enough.

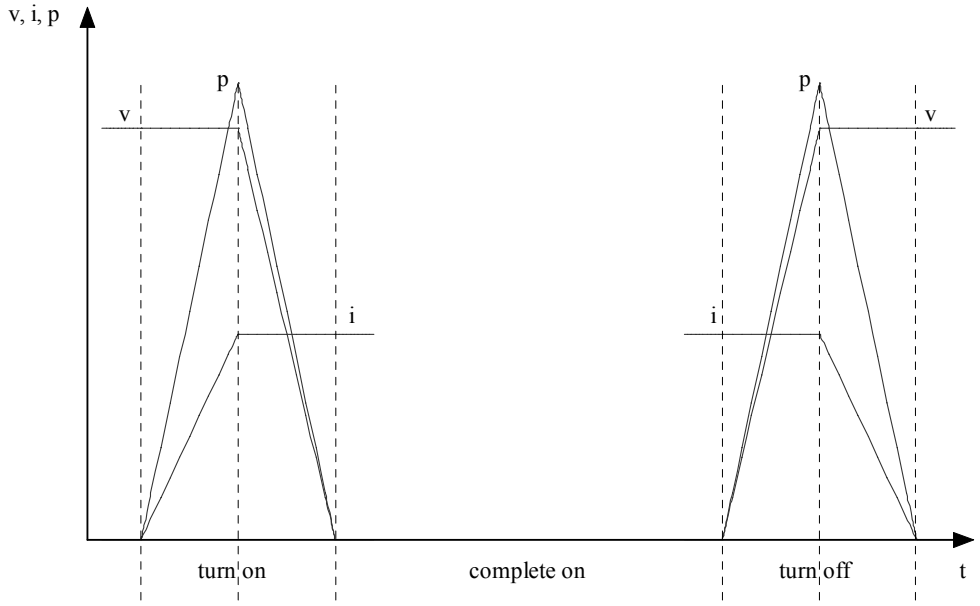


Figure 5.1 Switch Waveforms in Hard-Switched Converters

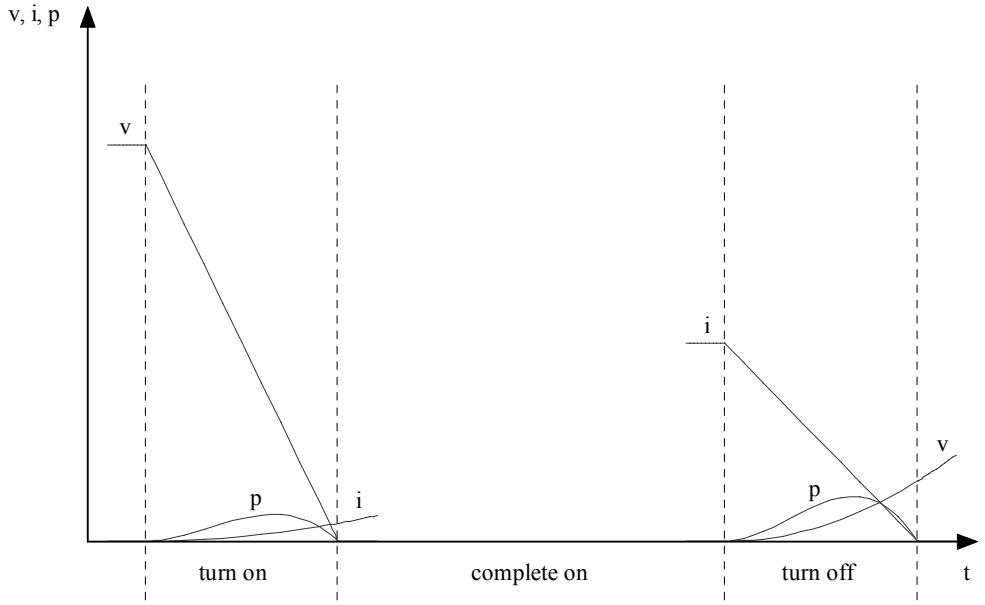


Figure 5.2 Switch Waveforms in Soft-Switched Converters

5.2 Categorization of the Soft-Switched Converters

According to the underlying operation principles of the resonant converters, they can be classified as shown in Figure 5.3, [47].

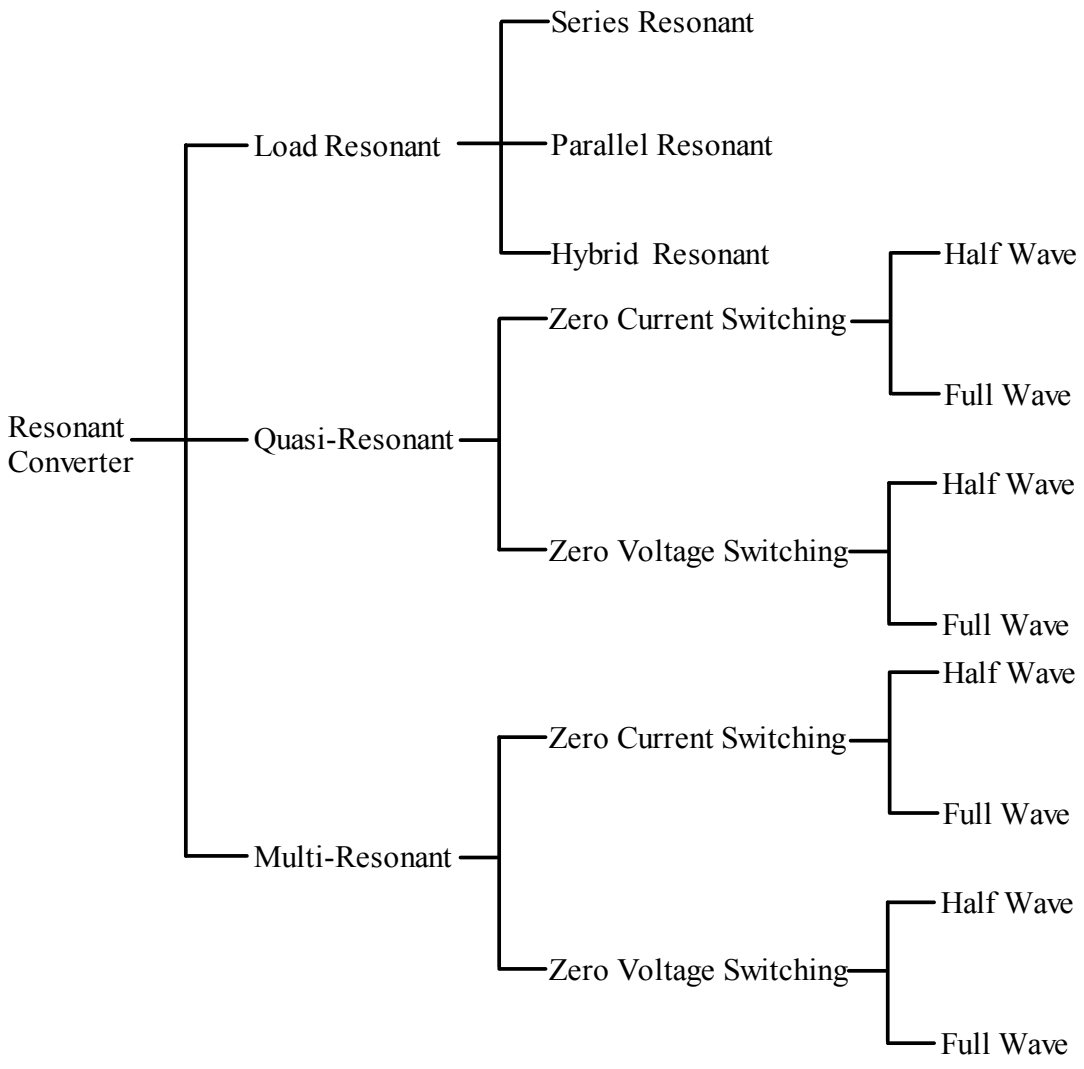


Figure 5.3 Categorization of Resonant Converters

Load-Resonant Converter, (LRC), includes a resonant tank leading to oscillating load voltage and current. According to the relative positions of the resonant tank

and the load, LRC can be characterised as Series-Loaded Resonant (SLR) Converter, Parallel-Loaded Resonant (PLR) Converter or Hybrid-Resonant Converter.

The resonant network of Quasi-Resonant Converter, (QRC), shapes the current or voltage waveform of the main switch. QRC is named because each switching period has resonant and non-resonant segments. This kind of converter is suitable for the operation in the low megahertz range and can be sub-classified as either Zero-Current Switching (ZCS) Converter or Zero-Voltage Switching (ZVS) Converter subject to the value which is zero when the switch turns on or off. In each sub-group of converters, different topology arrangements will result in either half wave or full wave version of the converter. Different types of QRCs are listed in detail in Appendix 9.

The fundamental principles of Multi-Resonant Converter, (MRC), are the same as QRC, expcept that the resonant operation is applied to both the main switches and output rectifier diodes. Because both of the switching losses in the main switches and the output diodes are reduced to the greatest extent, MRC is more suitable for very high frequency operation. It also has half wave and full wave versions as QRC.

The resonant half bridge dual converter introduced below is best classified to Half Wave Zero-Voltage Switching Quasi-Resonant Converters (HW-ZVS-QRC).

5.3 Topology

The topology of the resonant half bridge dual converter is shown in Figure 5.4. To achieve the resonant operation, three components are added to the topology of the basic half bridge dual converter shown in Figure 3.3(a): Inductor L_r, Capacitors C_1 and C_2. These, together with mosfets Q_1 and Q_2, form the elemental switching cells of the ZVS converter, [30] [48]. The inductor L_r, and the capacitors C_1 and C_2 may be composed in part, or entirely by the transformer leakage inductance and the output capacitances of the mosfets. Therefore, these parasitic components are actively exploited and completely absorbed into the resonant tank. During the turn off of the switch, the equivalent capacitor across the switch, either C_1 or C_2, resonates with the equivalent inductor, L_r, producing quasi-sinusoidal voltage and current waveforms. Consequently, turn on and turn off happen when the capacitor voltage is zero and a theoretically zero switching loss could be obtained. An important point of superiority of the ZVS arrangement over the ZCS arrangement is that in ZVS, the energy stored in the mosfet output capacitance can be returned to the circuit through the resonant action while in ZCS this capacitive energy is lost in the mosfet at turn on, [49]. This is especially true when the switching frequency approaches 500kHz and the capacitive loss becomes significant.

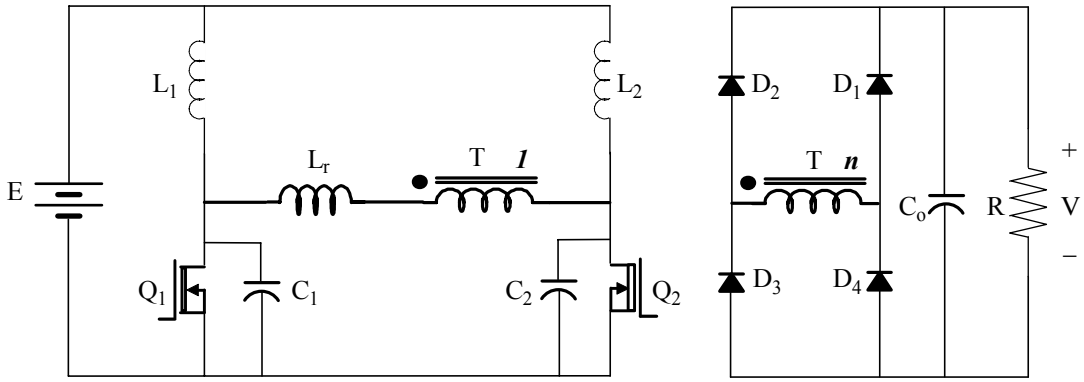


Figure 5.4 HW-ZVS Half Bridge Dual Converter

5.4 Resonance Condition Analysis for One Discontinuous Mode

The resonant half bridge dual converter is capable of several operational modes. The simplest mode, a discontinuous mode, is considered first.

The resonance of the converter can be analyzed using the equivalent circuit shown in Figure 5.5. L_r is the equivalent resonant inductor and C_1 and C_2 are equivalent resonant capacitors. D_{Q1} and D_{Q2} are embedded reverse body diodes of the mosfets. The current sources (I_0) model L_1 and L_2 in Figure 5.4. Voltage source V_d is the output capacitor voltage reflected to the primary side and diode D corresponds to the diodes D_1 to D_4 in the output full bridge rectifier. V_d and D reverse if the direction of i_{Lr} reverses. The effects of the transformer winding capacitance will be considered in due course.

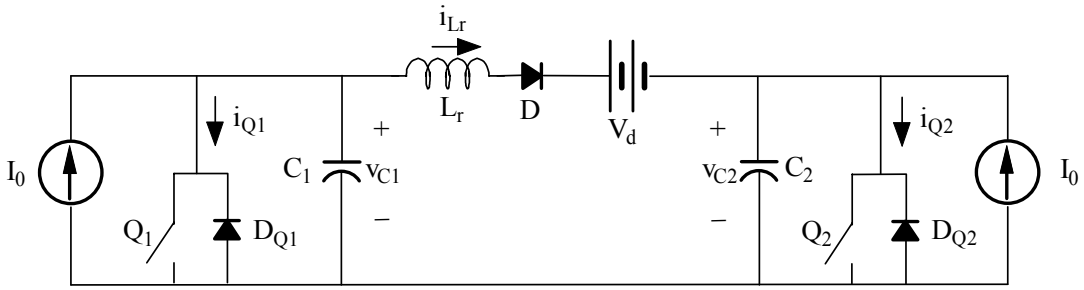


Figure 5.5 Equivalent Resonant Circuit

In order to analyze the switching behaviour of Q_1, the above equivalent circuit can be further simplified as shown in Figure 5.6. The resonant voltage and current waveforms for the discontinuous mode in one switching cycle are shown in Figure 5.7. The initial conditions at t_0 are that Q_1 and Q_2 are conducting, the current in the resonant inductor $i_{Lr}(t_0) = 0$ and the voltage across the resonant capacitor $v_{C1}(t_0) = 0$. The converter will proceed through the following four stages.

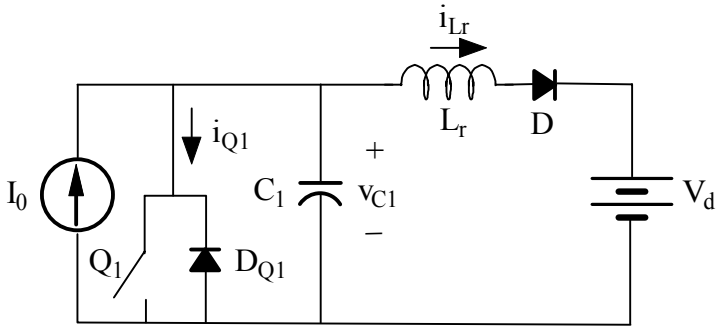


Figure 5.6 Simplified Equivalent Resonant Circuit

- Stage 1 ($t_0 \le t \le t_1$)

  In this stage, Q_1 turns off at time t_0. Because the initial capacitor voltage is zero, diode D is reversed biased. I_0 linearly charges the capacitor and the capacitor voltage v_{C1} is

$$v_{C1} = \frac{I_0}{C_1}(t - t_0) \tag{5.1}$$

- Stage 2 ($t_1 \le t \le t_4$)

  At t_1, the capacitor voltage reaches V_d and the diode D becomes forward biased. The capacitor voltage v_{C1} and the inductor current i_{Lr} are:

$$v_{C1} = V_d + I_0 Z_0 \sin \omega_0 (t - t_1) \tag{5.2}$$

$$i_{Lr} = I_0 - I_0 \cos \omega_0 (t - t_1) \tag{5.3}$$

  where $\omega_0 = \frac{1}{\sqrt{L_r C_1}}$ is the angular resonance frequency and $Z_0 = \sqrt{\frac{L_r}{C_1}}$ is the characteristic impedance. v_{C1} reaches its peak of $V_d + I_0 Z_0$ and i_{Lr} is I_0 at $t_2 = t_1 + \frac{\pi}{2\omega_0}$. And then at $t_3 = t_1 + \frac{\pi}{\omega_0}$, v_{C1} returns to V_d and i_{Lr} reaches its peak of $2I_0$. In order for the capacitor voltage v_{C1} to reach zero at t_4, $I_0 Z_0$ must be greater than V_d. This also sets the lower limit for the value of I_0 to

maintain the ZVS condition, once V_d and Z_0 are fixed. At t_4, v_{C1} is zero and i_{Lr} is I_4.

- Stage 3 ($t_4 \le t \le t_6$)

  At t_4 D_{Q1} or Q_1 turns on and the inductor current i_{Lr} is

$$i_{Lr} = I_4 - \frac{V_d}{L_r}(t - t_4) \tag{5.4}$$

  i_L linearly discharges to zero at t_6. The current in Q_1 would be the difference between I_0 and the inductor current. In the period from t_4 to t_5 the inverse mosfet diode, D_{Q1}, conducts as the remaining current in the inductor is greater than I_0. To achieve this condition it is required that $I_0 Z_0 > V_d$. The mosfet must be gated on during the interval from t_4 to t_5 to maintain a zero drain source voltage of Q_1. In this specific mode, it is also required that Q_2 stay on during this time interval.

- Stage 4 ($t_6 \le t \le t_7$)

  After t_6, i_{Lr} stays at zero until Q_2 turns off at t_7.

After t_7, the same cycle repeats for Q_2. The voltage and current waveforms of the capacitor C_2 and the inductor L_r reiterate the previous cycle but the inductor current is in the opposite direction.

The above discussion can be summarized in Table 5.1 and some important instantaneous values of the capacitor voltage and the inductor current are given in Table 5.2. A characteristic period for the discontinuous mode is [t_6, t_8], where the inductor current stays at zero.

Of course, the trade-offs of the soft-switched converter are higher switch ratings as mentioned before. The comparisons of the switching ratings for soft-switched and hard-switched half bridge dual converters are given in Table 5.3.

It is worth noting that in the HW-ZVS half bridge dual converter, in order to maintain the ZVS condition, the switching frequency must be selected against the circuit parameters and the input and load conditions, since the switch off-time and the switch duty cycle are determined by these parameters and conditions. It is mentioned before that mosfet Q_1 must turn on between t_4 and t_5 and these decide the switch off-time. Times t_4 and t_5 can be solved by Equations 5.2 and 5.4 and depends on the load current if the circuit parameters and the output voltage are fixed. According to Figure 3.4, the change in the input voltage will cause the change in the switch duty cycle. Therefore, to maintain the ZVS condition at different input and load conditions, variable switching frequency must be used.

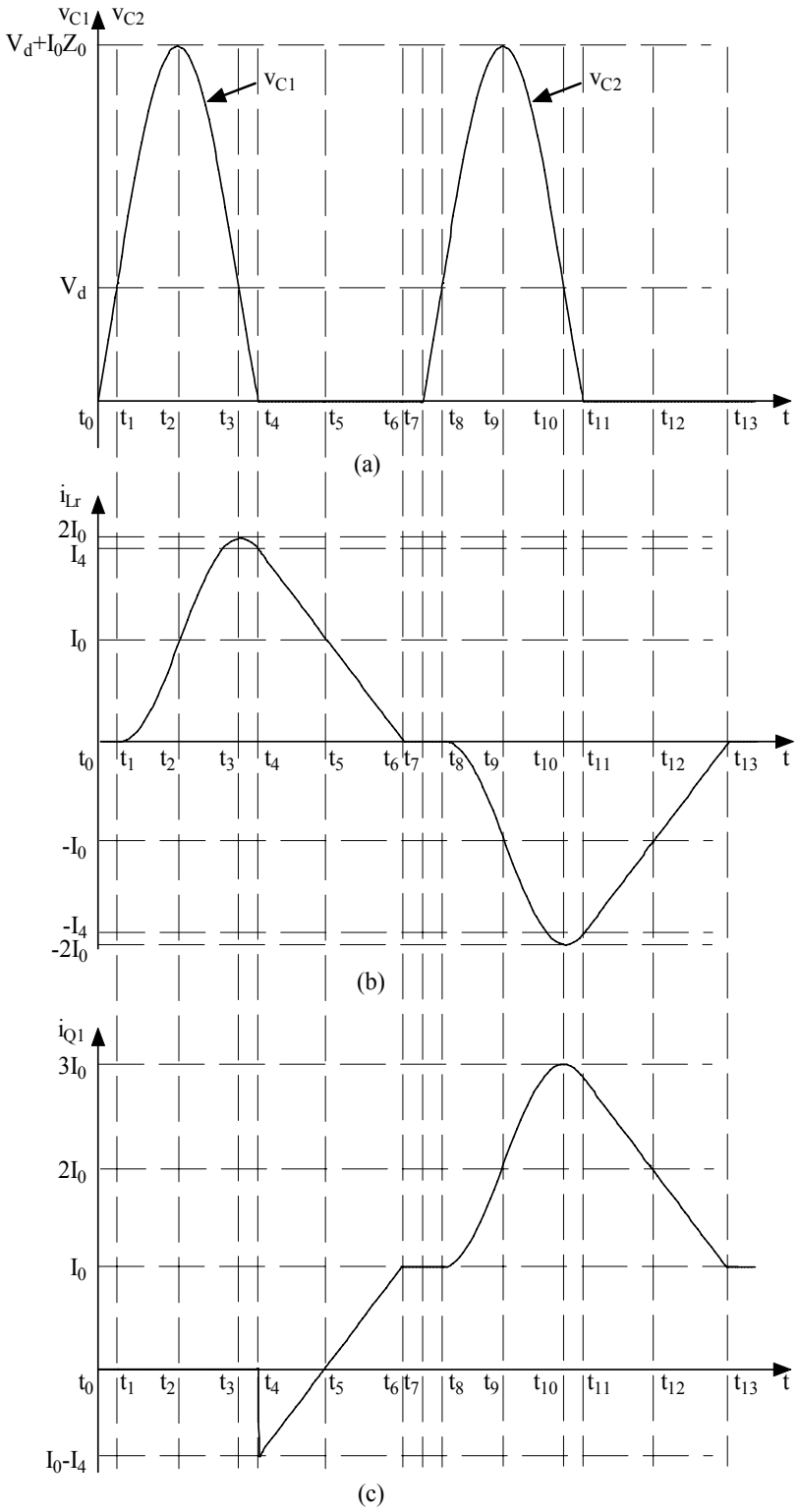


Figure 5.7 Theoretical Resonant Waveforms in One Discontinuous Mode (a) Capacitor Voltage (b) Inductor Current (c) Mosfet Current

Stage		Stage 1	Stage 2	Stage 3	Stage 4
Time Interval		$[t_0, t_1]$	$[t_1, t_4]$	$[t_4, t_6]$	$[t_6, t_7]$
Switching Actions	Q_1	Turns off at t_0	Stays off	D_{Q1} turns on at t_4, Q_1 must be turned on between t_4 and t_5	Stays on
	Q_2	Stays on	Stays on	Stays on	Stays on
Initial Conditions	v_{C1}	0	V_d	0	0
	i_{Lr}	0	0	I_4	0
Instantaneous Values	v_{C1}	$I_0(t-t_0)/C_1$	$V_d+I_0Z_0\sin\omega_0(t-t_1)$	0	0
	i_{Lr}	0	$I_0-I_0\cos\omega_0(t-t_1)$	$I_4- V_d(t-t_4)/L_r$	0

Table 5.1 Four Stages in the Discontinuous Mode

Time	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7
Event	Q_1 turns off	i_{Lr} is zero	v_{C1} peaks	i_{Lr} peaks	v_{C1} reaches zero	i_{Lr} reaches I_0	i_{Lr} reaches zero	Q_2 turns off
Capacitor Voltage v_{C1}	0	V_d	$V_d+I_0Z_0$	V_d	0	0	0	0
Inductor Current i_{Lr}	0	0	I_0	$2I_0$	I_4	I_0	0	0

Table 5.2 Waveform Parameters

Item	Soft-Switched Converter	Hard-Switched Converter
Peak Switch Voltage	$V_d+I_0Z_0$	V_d
Peak Switch Current	$3I_0$	$2I_0$

Table 5.3 Comparisons of the Switch Ratings

5.5 Different Operation Modes

As mentioned before, it has been identified that both continuous and discontinuous operation modes exist in the operation of the resonant half bridge dual converter. The following sections will discuss in detail all possible switching sequences and operation modes for this converter. The analysis will be based on the period from the turn on of Q_1 until the turn off of Q_2. The individual time points are as shown in Table 5.2.

5.5.1 Possible Switching Sequences

The half bridge dual converter requires that at least one of the two switches be on. Considering this prerequisite, the turn off of Q_2 must be preceded by the turn on of Q_1. Q_1 can turn on after its drain voltage reaches zero at t_4 and must be achieved by t_5, when Q_1 must conduct drain current, to maintain a zero drain voltage. Otherwise the available current charges the mosfet parallel capacitance and the zero turn on voltage condition is lost. This case is comparable to the ZVS converter operating in a less practical mode, full wave mode, where the switch turns off at a certain voltage

other than zero, [50] and a lower efficiency may result compared with the half wave operation of a same converter power level, [51].

As for Q_2, the turn off time, τ, can only fall into the following three time intervals, $[t_4, t_5]$, $[t_5, t_6]$ and $[t_6, \infty]$. Therefore, three possible switching sequences can be obtained by combining one possibility of Q_1's turn on interval and three possibilities of Q_2's turn off interval.

- Sequence I – Q_1 turns on between t_4 and t_5 and Q_2 turns off after t_6.
- Sequence II – Q_1 turns on between t_4 and t_5 and Q_2 turns off between t_5 and t_6.
- Sequence III – Q_1 turns on between t_4 and t_5 and Q_2 turns off between t_4 and t_5 but after Q_1 turns on. The mosfet Q_1 inverse diode is on when Q_2 turns off.

5.5.2 Continuous and Discontinuous Operation Modes

The first discontinuous mode discussed in Section 5.4 requires that mosfet Q_2 remain on until the inductor current falls to zero at t_6 to produce a prolonged period of zero inductor current. Other operational modes result if the turn off time of Q_2, τ, is advanced to the time before t_6. The following texts will analyze the boundary condition for continuous and discontinuous modes and their occurrence in each possible switching sequence. Initially the equivalent transformer winding capacitance is assumed to be zero and V_d reverses its polarity instantly when i_{Lr} reaches zero.

The converter can move through up to four states after Q_2 turns off as shown in Figure 5.8. Figure 5.8(a) shows the equivalent circuit when Q_2 turns off with non zero inductor current. In Figure 5.8(b), i_{Lr} reaches zero. If v_{C2} is still less than V_d, I_0 linearly charges C_2 until V_d is reached and the inductor current remains to be zero. The converter will bypass the state shown in Figure 5.8(b) if the initial inductor current was sufficiently high to cause v_{C2} to exceed V_d at the end of the state shown in Figure 5.8(a). In Figure 5.8(c), v_{C2} exceeds V_d and i_{Lr} is established in the negative direction. Figure 5.8(d) shows the equivalent circuit when D_{Q2} or Q_2 turns on after v_{C2} reaches zero and V_d linearly discharges L_r.

Assuming the initial conditions for the circuit shown in Figure 5.8(a) are $i_{Lr}(0) = \Delta_1 \cdot I_0$, $v_{C2}(0) = 0$ and those for the circuit shown in Figure 5.8(c) are $i_{Lr}(0) = 0$, $v_{C2}(0) = \Delta_2 \cdot V_d$, where $\Delta_1 \geq 0$ and $\Delta_2 \geq 1$, the capacitor voltage v_{C2} and inductor current i_{Lr} in Figure 5.8(a) would be

$$v_{C2}(t) = (1+\Delta_1) I_0 Z_0 \sin(\omega_0 t) + V_d \cos(\omega_0 t) - V_d \tag{5.5}$$

$$i_{Lr}(t) = -\frac{V_d}{Z_0} \sin(\omega_0 t) + (1+\Delta_1) I_0 \cos(\omega_0 t) - I_0 \tag{5.6}$$

and in Figure 5.8(c) would be

$$v_{C2}(t) = I_0 Z_0 \sin(\omega_0 t) - (1-\Delta_2) V_d \cos(\omega_0 t) + V_d \tag{5.7}$$

$$i_{Lr}(t) = (1-\Delta_2)\frac{V_d}{Z_0}\sin(\omega_0 t) + I_0\cos(\omega_0 t) - I_0 \tag{5.8}$$

where $\omega_0 = \frac{1}{\sqrt{L_r C_2}}$ is the angular resonance frequency and $Z_0 = \sqrt{\frac{L_r}{C_2}}$ is the characteristic impedance of the resonant tank.

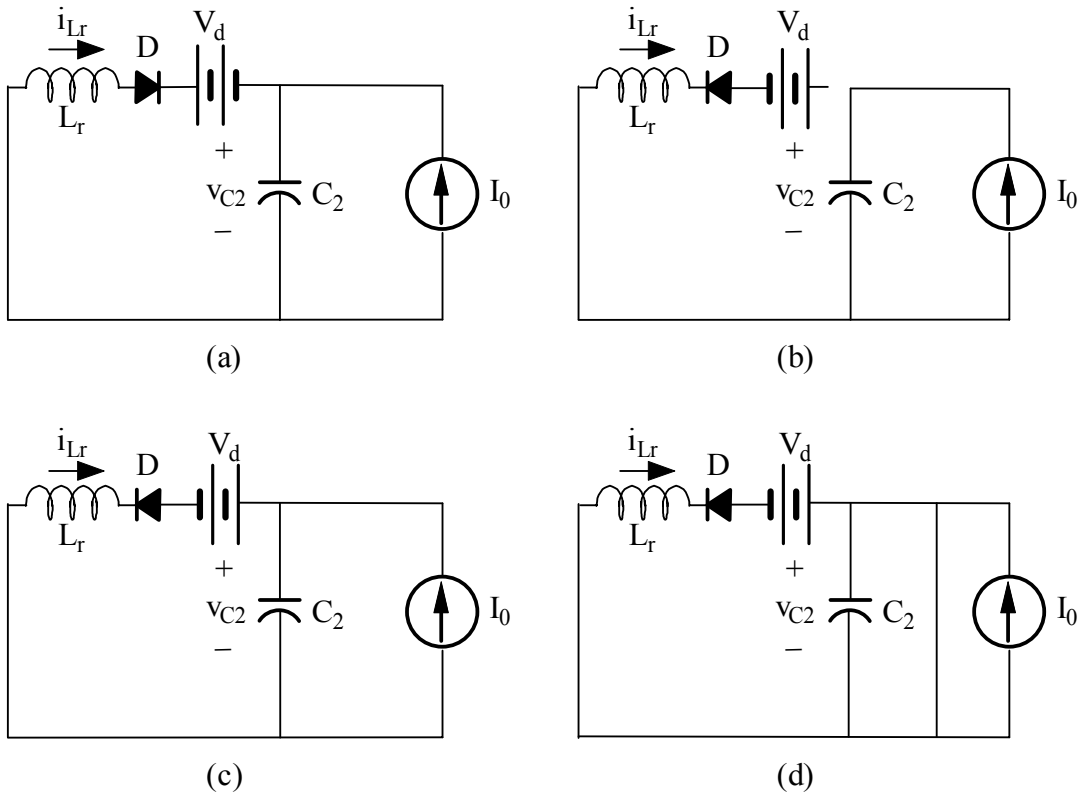


Figure 5.8 Four Possible Configurations

According to the continuity of the current in the resonant inductor, the operation of the converter can be classified as continuous or discontinuous mode. Due to the existence of the series diode D and its different polarities under different polarities of the voltage source V_d, the current behaviour of the resonant inductor fully

depends on the capacitor voltage $v_C(t)$ at $i_{Lr} = 0$. If $v_C(t) \geq V_d$, then D is forward biased and the converter runs in the continuous mode. Otherwise, if $v_C(t) < V_d$, D is reverse biased and i_{Lr} stays at zero until the resonant capacitor voltage charges to V_d. In this case, the converter experiences an extended zero inductor current period and runs in the discontinuous mode.

Assuming the load condition is $I_0 Z_0 = k \cdot V_d$ and $B = (1 + \Delta_1)k$, the electrical angle when i_{Lr} reaches zero according to Equation 5.6 is

$$\omega_0 t(i_{Lr} = 0) = \cos^{-1} \frac{k}{\sqrt{1 + B^2}} - \tan^{-1} \frac{1}{B} \tag{5.9}$$

Substituting $\omega_0 t$ from Equation 5.9 into Equation 5.5 yields

$$v_{C2}(i_{Lr} = 0) = (\sqrt{1 + B^2 - k^2} - 1) \cdot V_d \tag{5.10}$$

For the continuous mode operation

$$(\sqrt{1 + B^2 - k^2} - 1) \cdot V_d \geq V_d \text{, i.e. } \Delta_1 \geq \frac{\sqrt{k^2 + 3}}{k} - 1 .$$

Figure 5.9 shows $f(k) = \frac{\sqrt{k^2+3}}{k} - 1$, the boundary function plotted against the load and timing factors k and Δ_1 to show the conditions for continuous and discontinuous modes.

The following discussion about different operation modes in three possible switching sequences is based on adjusting the turn off time of Q_2, τ, to occur before t_7 as shown in Figure 5.7. Resonant waveforms are shown, assuming that turn on of Q_1 happens at t_4, the exact time when v_{C1} reaches zero. The markings on the time axis are as shown in Table 5.2.

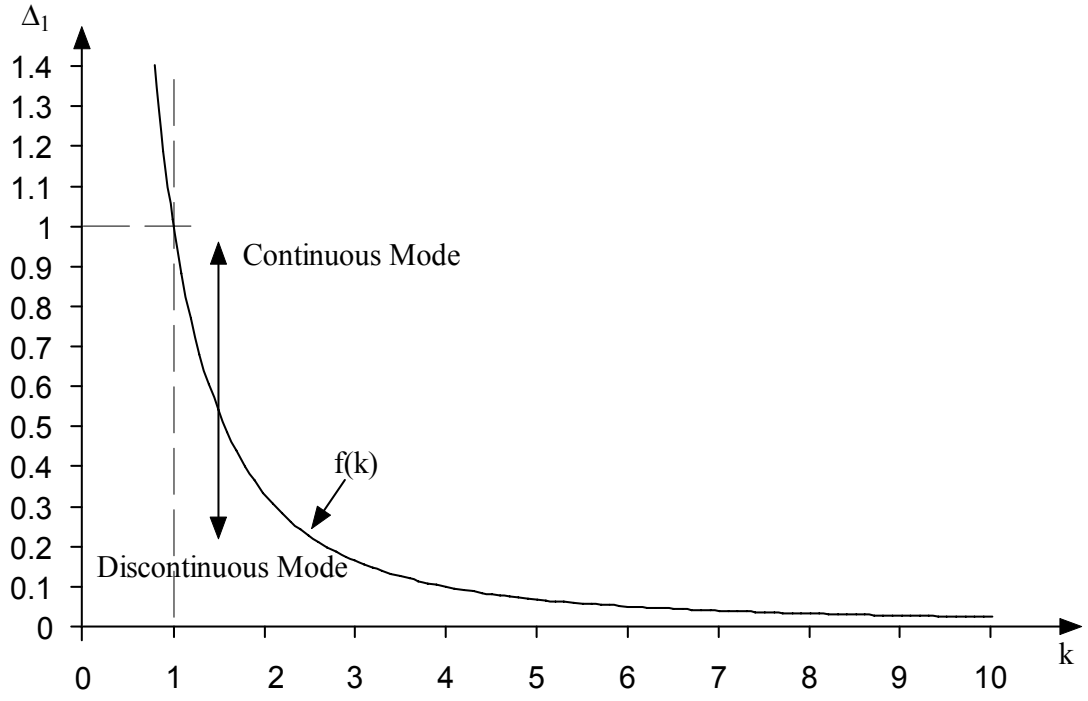


Figure 5.9 Boundary for Continuous and Discontinuous Modes

- Sequence I ($t_6 < \tau < t_7$)

  In this sequence, turn off is advanced but still after t_6. The converter still runs in the discontinuous mode due to the extended period of zero inductor current. There are no distinctions between the resonant waveforms in this sequence and in Section 5.4, except for a curtailed zero inductor current period.

- Sequence II ($t_5 < \tau < t_6$)

  In this sequence, turn off is advanced to the time interval $[t_5, t_6]$. The converter is capable of running in both continuous and discontinuous modes. In order to show different inductor current waveforms, the load condition, $I_0Z_0 = 1.4V_d$, is selected. In this specific case, the boundary value for the continuous and the discontinuous modes is $\Delta_1 = 0.59$. Figures 5.10 and 5.11 respectively show the voltage and current waveforms in discontinuous mode, based on $\Delta_1 = 0.2$, and in continuous mode, based on $\Delta_1 = 0.8$. In the discontinuous operation mode, prolonged zero value periods, $[t_1, t_1']$ and $[t_8, t_8']$, exist in the inductor current waveform.

- Sequence III ($t_4 < \tau < t_5$)

  In this sequence, turn off is advanced to the time interval of $[t_4, t_5]$.

It is mentioned in Section 5.4 that critical to the successful operation of the resonant half bridge dual converter, it is required that $I_0Z_0 \geq V_d$, or $k \geq 1$. To

be more accurate, the load factor k has to fulfil $k^2 + (1-\Delta_2)^2 \geq 1$ according to Equation 5.7. Otherwise, the voltage across the switch cannot naturally drop to zero. To ease the difficulties in the design process, this condition is always simplified as $k \geq 1$. Without this simplification, whether the switch voltage falls back to zero can only be determined by the trial and error method.

Because $\Delta_1 \geq 1$ and $f(k) \leq 1$ is always true in this switching sequence and for $k \geq 1$, the converter always runs in the continuous mode. The voltage and current waveforms, based on $\Delta_1 = 1.2$, are shown in Figure 5.12. Mathematic manipulations verify that the continuous operation mode in Sequence III is characterized by a shorter inductor linear discharging period and higher peak values in the resonant capacitors and inductor, compared with the continuous mode in Sequence II.

Table 5.4 shows different states in Figure 5.8 which the above sequences include. Similar switching options can be obtained for Q_2's turn on and Q_1's turn off.

Sequence and Mode	State (a)	State (b)	State (c)	State (d)
Sequence I – Discontinuous Mode		✓	✓	✓
Sequence II – Continuous Mode	✓		✓	✓
Sequence II – Discontinuous Mode	✓	✓	✓	✓
Sequence III – Continuous Mode	✓		✓	✓

Table 5.4 Different Operation Modes

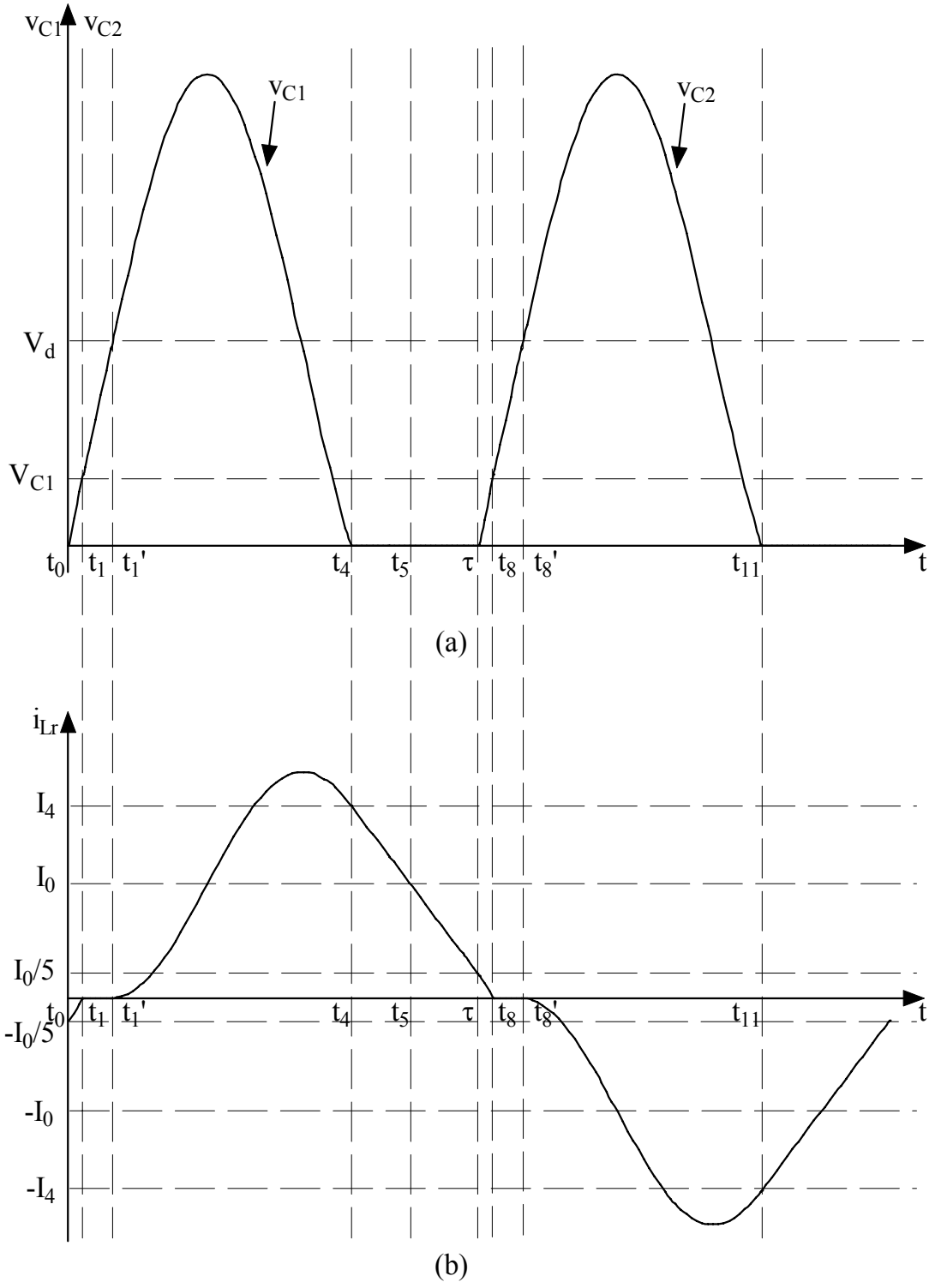


Figure 5.10 Discontinuous Operation Mode in Sequence II ($\Delta_1 = 0.2$) (a) Capacitor Voltage (b) Inductor Current

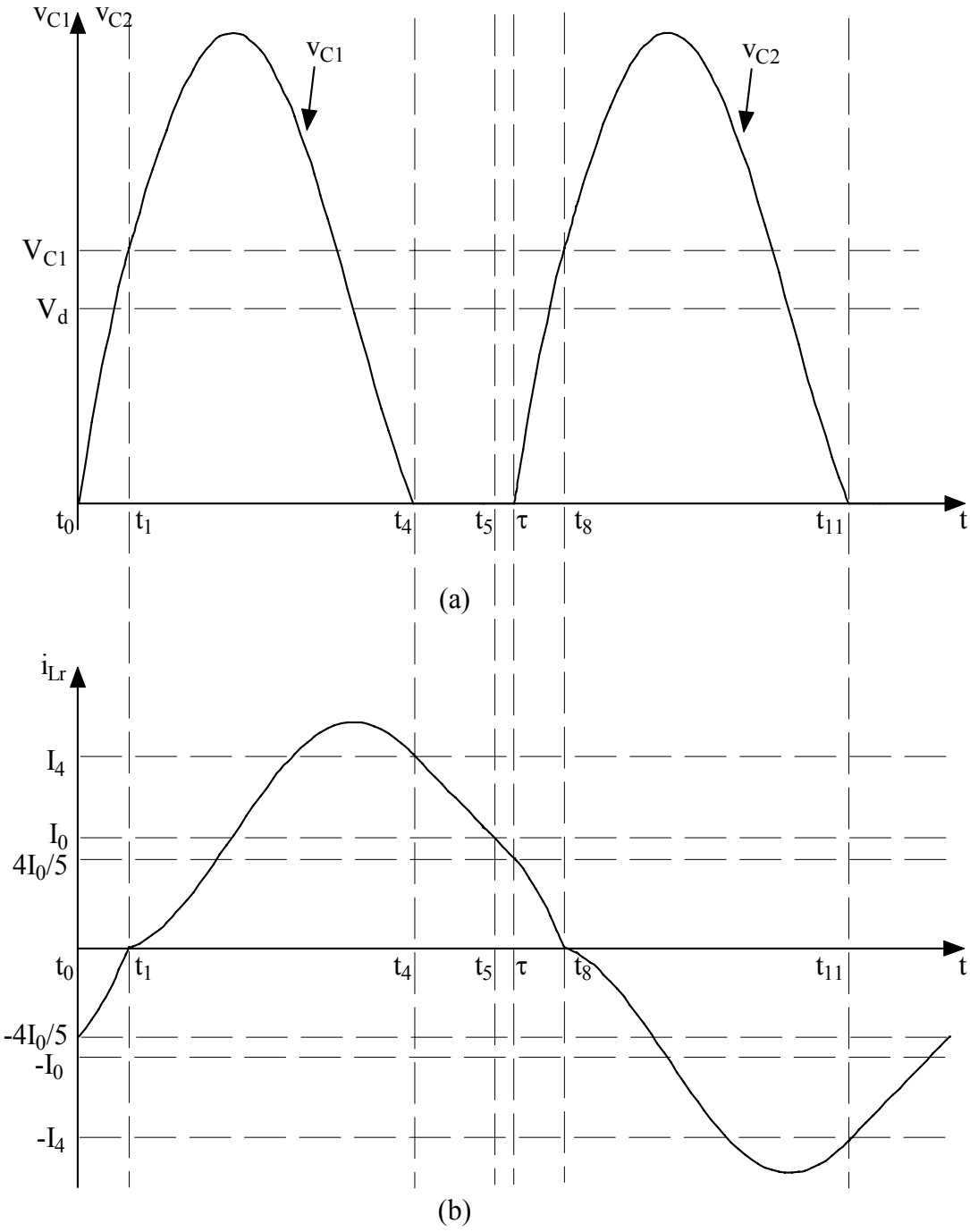


Figure 5.11 Continuous Operation Mode in Sequence II ($\Delta_1 = 0.8$) (a) Capacitor Voltage (b) Inductor Current

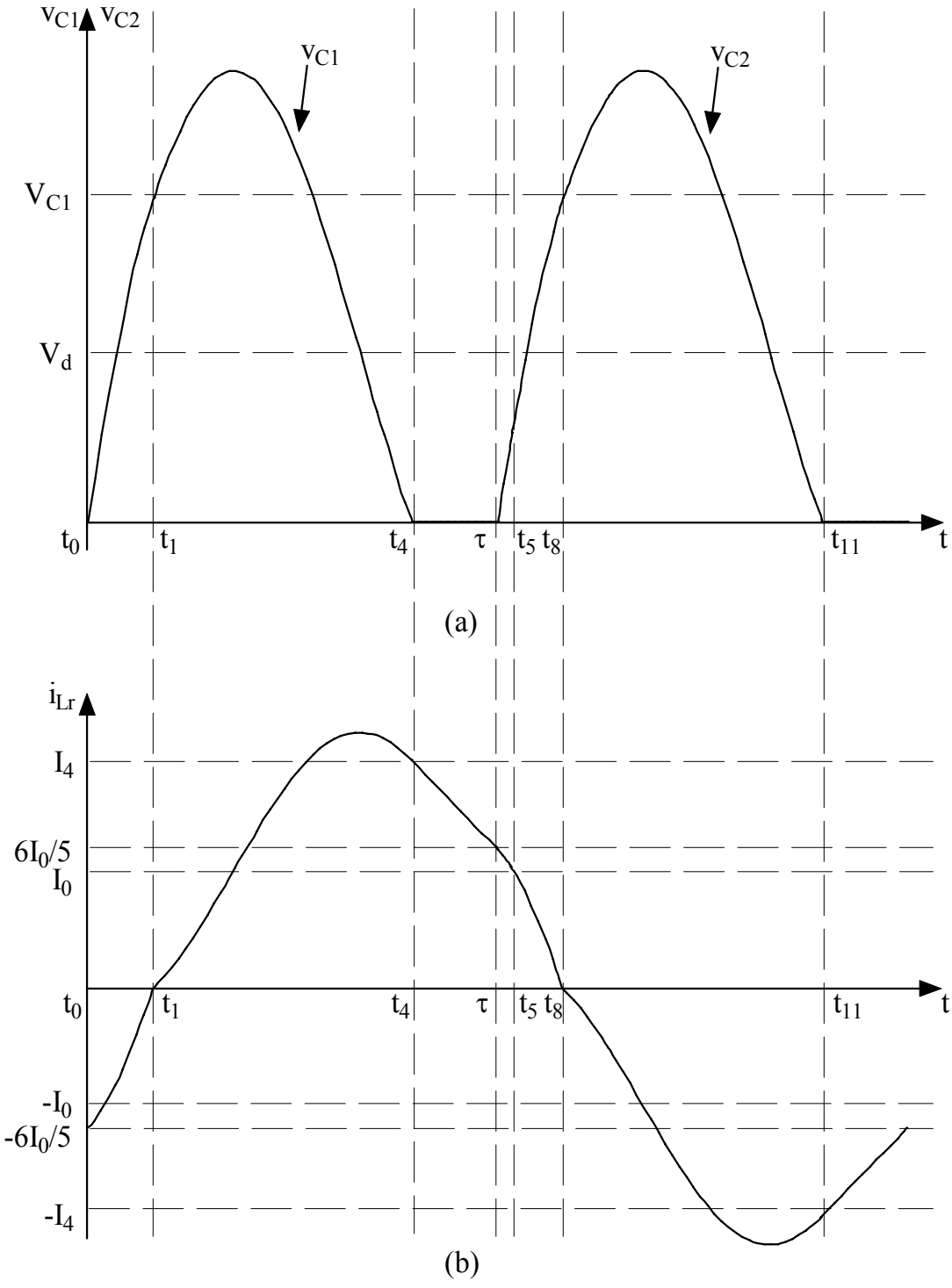


Figure 5.12 Continuous Operation Mode in Sequence III ($\Delta_1 = 1.2$) (a) Capacitor Voltage (b) Inductor Current

5.6 Transformer Winding Capacitance

Like many series resonant topologies where the transformer and rectifier are current fed, this topology is tolerant of winding and diode capacitance. If winding capacitance is considered then the reversal of the transformer primary voltage will not happen instantly after i_{Lr} reaches zero. A consequence is that the abrupt change in conductor current slope at the zero crossing, t_8 in Figures 5.11 and 5.12 will be removed. Figure 5.13 shows the equivalent circuit during the primary voltage transition period.

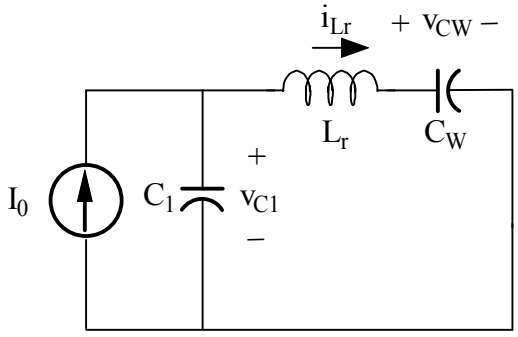


Figure 5.13 Equivalent Circuit during Voltage Transition

Assuming the initial conditions are $i_{Lr}(0) = 0$, $v_{C1}(0) = \Delta_2 \cdot V_d$ and $v_{CW}(0) = -V_d$, the inductor current, the capacitor C_1 voltage and the capacitor C_w voltage would be

$$i_{Lr}(t) = \frac{C_W I_0}{C_1 + C_W}\left[1 - \cos(\omega_0' t)\right] + \frac{(1+\Delta_2)V_d}{Z_0'}\sin(\omega_0' t) \qquad (5.11)$$

$$v_{C1}(t) = \frac{V_d}{C_1 + C_W}\left[C_W(1+\Delta_2)\cos(\omega_0' t) + C_1\Delta_2 - C_W\right]$$

$$+ \frac{C_W I_0 Z_0'}{(C_1 + C_W)^2}\left[C_1\omega_0' t + C_W \sin(\omega_0' t)\right] \qquad (5.12)$$

$$v_{CW}(t) = \frac{V_d}{C_1 + C_W}\left[C_1\Delta_2 - C_W - C_1(1+\Delta_2)\cos(\omega_0' t)\right]$$

$$+ \frac{C_1 C_W I_0 Z_0'}{(C_1 + C_W)^2}\left[\omega_0' t - \sin(\omega_0' t)\right] \qquad (5.13)$$

where $\omega_0' = 1\Big/\sqrt{\frac{C_1 C_W}{C_1 + C_W}\cdot L_r}$ is the angular resonance frequency and $Z_0' = \sqrt{L_r\Big/\frac{C_1 C_W}{C_1 + C_W}}$ is the characteristic impedance. The qualitative effect of the introduction of the transformer winding capacitance is that a new resonant tank is formed by the transformer leakage inductance and the series equivalent of the mosfet parallel capacitance and the transformer winding capacitance. This can be verified by the new angular resonance frequency and the new characteristic impedance of the resonant tank.

Equation 5.13 shows that the voltage across the transformer reverses at a controlled rate due to the effect of the transformer winding capacitance. Differentiation of Equation 5.13 at t = 0 also shows a zero first derivative. The winding voltage transition is slow initially and this provides a soft-switching condition for the diodes in the rectifier at turn off, resulting in lower power losses associated with the diodes.

In the practical implementations, C_w would be the parallel capacitance of transformer winding capacitance and the rectifier diode junction capacitance. There are limits to the allowable levels of capacitance – a winding capacitance of a quarter of the resonant capacitance will not significantly alter the converter operation. However, in series resonant converter applications, larger capacitances will lead to higher component stresses in the resonant tank, as a trade-off of the soft-switching feature in the diodes, [52].

5.7 Experimental Results of One Continuous Mode

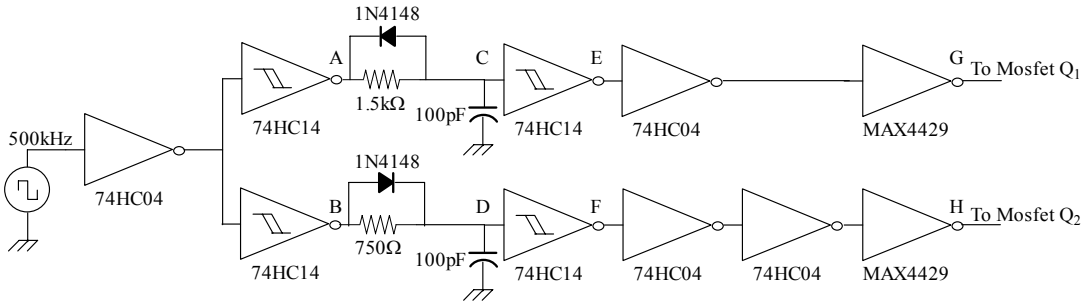
To verify the theoretical discussion, a 1MHz resonant half bridge dual converter was constructed for one of the continuous operational modes. A photo of the experimental converter is given in Appendix 7.

5.7.1 Driving Circuit

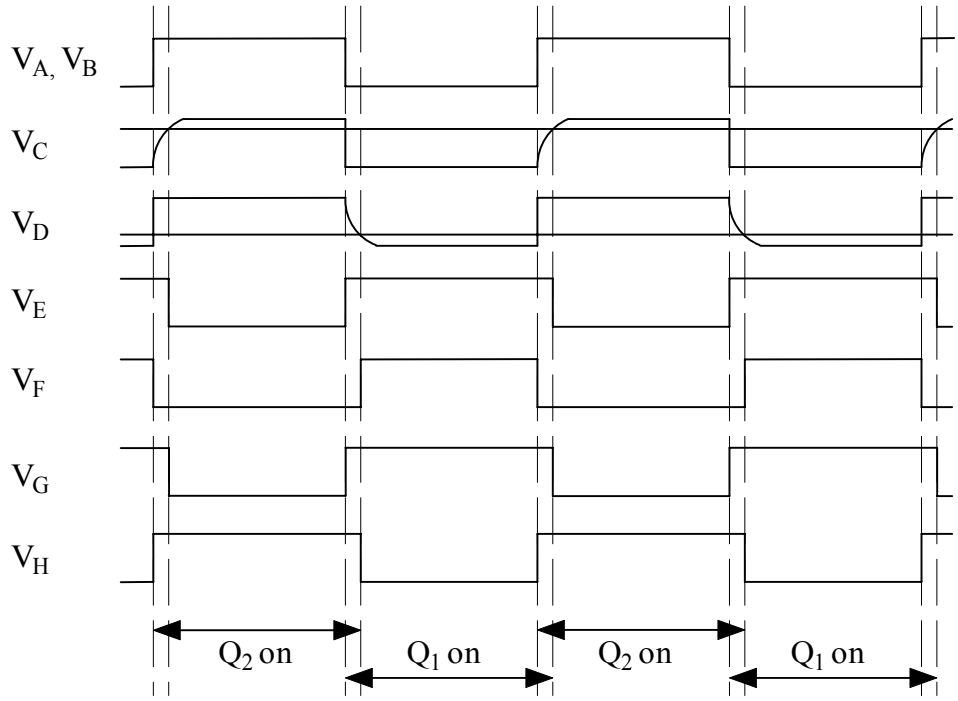
With a maximum oscillation frequency of 350kHz, LM3524D is not qualified for the task of providing a 500kHz mosfet gate driving signal to the resonant half bridge dual converter. A new driving circuit was built, as shown in Figure 5.14(a).

A 500kHz square wave source is used and it goes through several high speed CMOS inverters and schmitt triggers. The purpose of the network made up of one resistor, one diode and one capacitor between A and C or B and D is to generate a switch duty cycle slightly greater than 50% or to provide an overlap of the on state of the

two mosfets. The final output stage of the driving circuit still employs two MAX4429s to provide high current gate driving signals. The voltage waveform at each point is shown in Figure 5.14(b). The duty cycle of each mosfet can be easily adjusted within a small range by adjusting two resistances to offer different time constants for charging and discharging of two capacitors.



(a)



(b)

Figure 5.14 Driving Circuit (a) Schematic (b) Voltage Waveforms

5.7.2 Design Process

The design process of Inductors L_1 and L_2, Transformer T, Mosfets Q_1 and Q_2, Diodes D_1 to D_4 and Capacitor C_o is similar to that of the hard-switched converters. However, the new components in the resonant tank of this converter must be carefully designed to meet the ZVS basic requirement of $k \geq 1$.

Several other design considerations are worthy to be highlighted here.

- Skin effects are significant in this design. The penetration depth given in [27] is

$$\Delta = k_{\Delta} f_s^{-1/2} \tag{5.14}$$

where $k_{\Delta} = 72 mmHz^{1/2}$ for copper conductor at 70°C. From Equation 5.14, the penetration depth is 0.10mm at 500kHz, the transformer and inductor excitation frequency. Therefore Litz wire must be used to obtain a low copper loss in both the transformer and the resonant inductor.

- In the resonant circuit, resonant capacitors are required to be connected across the mosfet drain and source. High frequency parasitic oscillations, at frequencies up to 50MHz were observed during the experimentation,

due to the Equivalent Series Inductance (ESL) of the resonant capacitors as well as the stray inductance of the leads and tracks connecting the capacitors and the mosfets. Considering the size of the mosfets, physically small capacitors are preferred because they can be paralleled with mosfets using shorter leads and tracks. Other solutions include paralleling several capacitors to achieve a low effective stray inductance. In the implementation of the resonant capacitors in this converter, seven monolithic ceramic capacitors are used in parallel with the mosfets on each side due to their small size and low ESL, [53]. A bonus of this design is that ceramic capacitors offer extremely low Equivalent Series Resistance (ESR) and therefore less intrinsical power loss in the resonant capacitors, [54].

- As a trade-off of the low switching loss in mosfets under the resonant switching arrangement, the voltage and current ratings of mosfets could be significantly higher than those in the hard-switched converters. A direct impact of higher mosfet voltage ratings is higher forward resistance and consequently higher conduction loss for the same current level. Therefore, two mosfets are paralleled to achieve a lower effective $R_{DS(on)}$ in this converter in order that the decrease in the switching loss would not be offset by the increase in the conduction loss in mosfets.

The components used in the converter are:

- Inductors L_1 and L_2 – Core type Siemens RM10, ferrite grade Siemens N48, total air gap = 0.21mm, number of turns = 13, wire diameter 1.00mm (1.06mm overall).
- Transformer T – Core type Philips ETD29, ferrite grade Neosid F44, primary wire: Litz wire made up of 34 strands of fine wires, secondary wire: Litz wire made up of 8 strands of fine wires, fine wire diameter 0.11mm (0.135mm overall), primary number of turns = 12, secondary number of turns = 128.
- Additional Resonant Inductor L_a – Core type Philips ETD39 gapped, ferrite grade Philips 3C90, Litz wire made up of 34 strands of fine wires, fine wire diameter 0.11mm (0.135mm overall), number of turns = 6.
- Additional Resonant Capacitors C_{a1} and C_{a2} – 1.5nF ceramic capacitor, V_{dc} = 250V.
- Mosfets Q_1 and Q_2 – Intersil RFP40N10, V_{DS} = 100V, I_D = 40.0A, $R_{DS(on)}$ = 0.040Ω.
- Diodes D_1 to D_4 – ST STTA106U, V_{RRM} = 600V, I_F = 1A, V_F = 1.5V, t_{rr} = 20ns;
- Capacitor C_o – Philips MKP capacitor 1μF.

Some of the key values used in the resonant tank are:

- Additional Resonant Inductance L_a = 4.5μH;
- Transformer Leakage Inductance $L_{leakage}$ = 0.34μH;
- Additional Resonant Capacitance $C_{a1} = C_{a2}$ = 10.5nF;

- Mosfet Output Capacitance C_{oss} = 0.5nF;
- I_0 = 2.35A, E = 20V, V_d = 34V;
- C_w = 2.8nF (referred to the primary side).

From the values listed above, the equivalent resonant inductance can be calculated as 4.84μH and the equivalent resonant capacitance can be calculated as 11nF. Therefore, the load condition is k = 1.4.

5.7.3 Comparisons of Theoretical and Experimental Waveforms

A specific switching arrangement, where Q_1 turns on at t_4 and Q_2 turns off at t_5, is selected in the experiment. According to Figure 5.7, Q_1 turns on when the capacitor voltage is zero and Q_2 turns off when the inductor current is I_0. The boundary condition given in Section 5.5.2 shows that the converter runs in the continuous mode under the selected conditions of $\Delta_1 = 1$ and k = 1.4. In order to evaluate the experimental results, a theoretical analysis is conducted for this specific case first.

Form Figure 5.7, we can easily know that at t_5, the inverse diode of Q_1, D_{Q1}, stops conducting and the initial conditions are $i_{Lr}(t_0) = I_0$ and $v_{C2}(t_0) = 0$. For the convenience in drawing and discussing quantitatively the voltage and current waveforms of the resonant inductor and capacitors, the counterpart of the above period will be discussed. Four stages after the turn off of Q_1 (Q_1 turns off when the inverse diode of Q_2 stops conducting) are shown in Figure 5.15. The current and

voltage waveforms are shown in Figure 5.16. The markings on the time axis are as shown in Table 5.2.

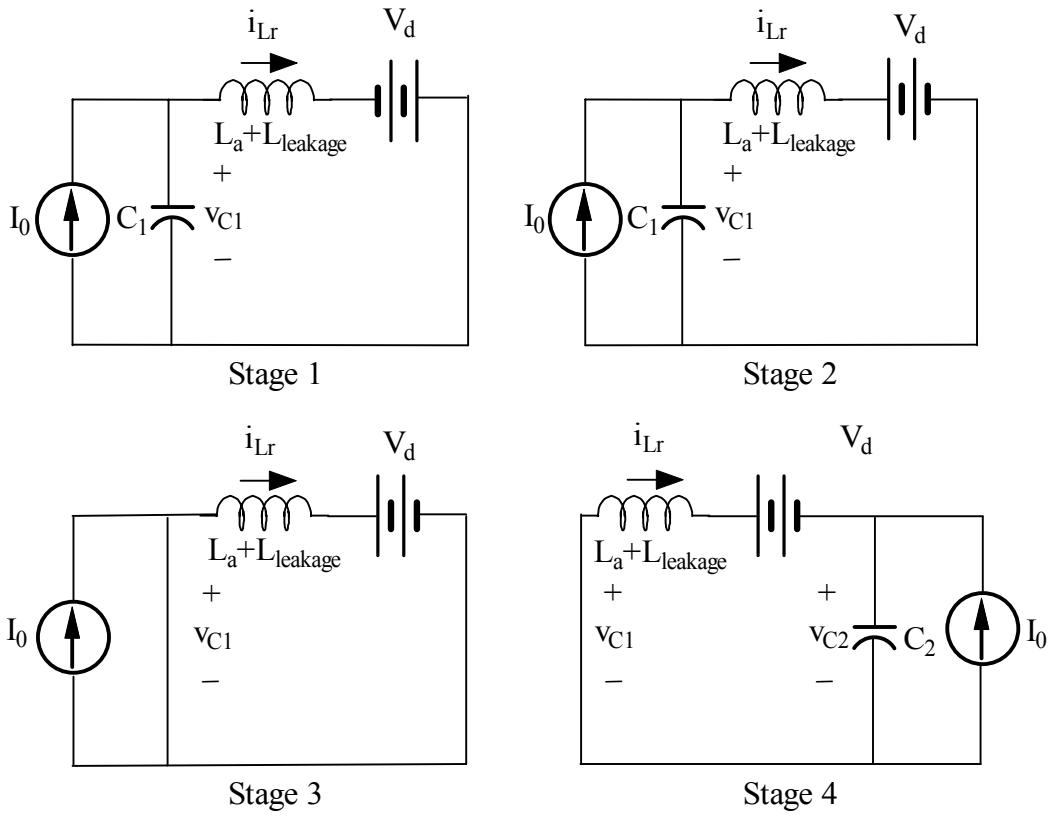


Figure 5.15 Equivalent Circuits of Four Stages in the Continuous Mode

- Stage 1 ($t_0 \le t \le t_1$): The initial conditions of this stage are $i_{Lr}(t_0) = -I_0$ and $v_{C1}(t_0) = 0$. The mosfet Q_1 turns off at t_0 and C_1 rapidly charges under the influence of the current source and the initial inductor current. The capacitor voltage v_{C1} and the inductor current i_{Lr} are:

$$v_{C1} = 2I_0 Z_0 \sin\omega_0(t-t_0) + V_d \cos\omega_0(t-t_0) - V_d \qquad (5.15)$$

$$i_{Lr} = \frac{V_d}{Z_0}\sin\omega_0(t-t_0) - 2I_0\cos\omega_0(t-t_0) + I_0 \qquad (5.16)$$

This period ends when the inductor current reaches zero. This point depends on the magnitude of I_0Z_0 relative to V_d. At $I_0Z_0 = 1.4V_d$, the inductor current reaches zero at $\omega_0 t_1 = 42.3°$. The corresponding capacitor voltage $V_{C1} = 1.6V_d$.

- Stage 2 ($t_1 \le t \le t_4$): The initial conditions of this stage are $i_{Lr}(t_1) = 0$ and $v_{C1}(t_1) = 1.6V_d$. At the beginning of this stage, V_d reverses its polarity as shown in Figure 5.15. The analysis here does not consider the effect of parasitic capacitances and this reflected transformer voltage reverses instantaneously. Because the initial voltage across the capacitor is greater than V_d, the capacitor and the inductor resonate and the inductor current is established in the positive direction. For the parameters selected, the capacitor voltage v_{C1} and the inductor current i_{Lr} are:

$$v_{C1} = I_0Z_0\sin\omega_0(t-t_1) + 0.6V_d\cos\omega_0(t-t_1) + V_d \qquad (5.17)$$

$$i_{Lr} = \frac{0.6V_d}{Z_0}\sin\omega_0(t-t_1) - I_0\cos\omega_0(t-t_1) + I_0 \qquad (5.18)$$

The capacitor voltage peaks at $2.5V_d$ and returns to zero at $\omega_0 t_4 = 239°$. At this point the inductor current $I_4 = 1.8I_0$.

- Stage 3 ($t_4 \le t \le t_5$): The initial conditions of this stage are $i_{Lr}(t_4) = 1.8I_0$ and $v_{C1}(t_4) = 0$. At t_4, Q_1 turns on and the inductor current i_{Lr} is

$$i_{Lr} = 1.8I_0 - \frac{V_d}{L_r}(t - t_4) \tag{5.19}$$

  where $L_r = L_a + L_{leakage}$, L_a is the additional resonant inductance and $L_{leakage}$ is the transformer leakage inductance. The inductor current linearly declines to I_0 at t_5, when Q_2 turns off.

- Stage 4 ($t \ge t_5$): Q_2 turns off at t_5 and the above cycle repeats for Q_2.

The Equations 5.15 to 5.18 for the resonant voltage and current shown here are in fact the simplified forms of Equations 5.5 to 5.8, with known values of $\Delta_1 = 1$ and $\Delta_2 = 1.6$, applied to the period after the turn off of Q_1. The only difference is that i_{Lr} must be reversed because the turn off of Q_1 is considered here, not the turn off of Q_2 as in Equations 5.5 to 5.8.

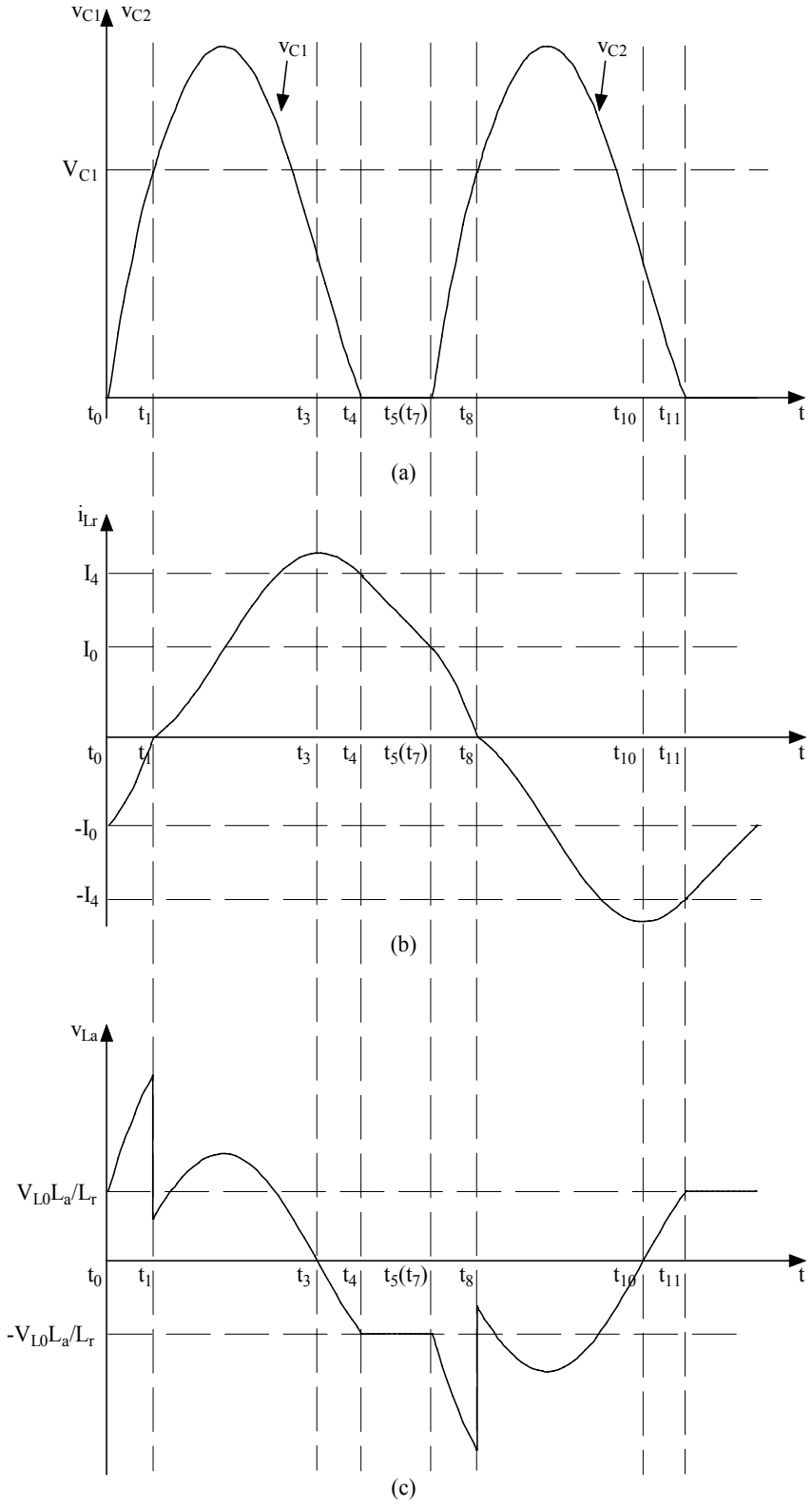


Figure 5.16 Theoretical Resonant Waveforms in One Continuous Mode (a) Capacitor C_1 Voltage (b) Inductor L_r Current (c) Inductor L_a Voltage

Figure 5.17 shows the experimental waveforms in the above continuous mode. The experimental results in Figures 5.17(a), (b) and (c) compare very favorably with the predicted results in Figure 5.16. In Figure 5.17(a), mosfet Q_1 gate driving signal was recorded as Channel 2 waveform to verify zero voltage turn on. However, the parasitic capacitance does affect the experimental results with regard to the transformer voltage reversal after t_1 shown in Figure 5.16. This transition is not instantaneous, as shown in Figure 5.17(d), and the change in inductor current slope at the zero crossing is less severe than the analytical solution suggests. In this case the winding capacitance is a quarter of the resonant capacitance and this means the winding voltage takes approximately 100ns to reverse. By comparison, the reverse recovery time, t_{rr}, for the output diode is 20ns. No reverse recovery problem is visible in the diode voltage waveform shown in Figure 5.17(e). In this case, the experimental waveforms are virtually free from parasitic oscillations. All of the parasitic components are captured by the normal converter operations. It is worthwhile noting that this converter achieves the direct rectification of a 1MHz waveform at 360V. This is regarded to be a very significant feat. Even minor reverse recovery losses can easily lead to thermal runaway in the diodes. This was observed with Fairchild UF4004 diodes which have a maximum reverse recovery time of 50ns and were used in some early experimental work.

Figure 5.17 Experimental Waveforms (a) Mosfet Q_1 Drain Voltage (Ch1) and Gate Waveform (Ch2) (b) Inductor L_a Current (c) Inductor L_a Voltage (d) Transformer T Primary Voltage (e) Diode D_3 Voltage

Table 5.5 compares some key waveform parameters. The differences between the calculated and experimental values are believed to be due to the effect of transformer parasitic capacitance.

Parameter	Calculated Value	Experimental Value
$V_{C1}(t_1)$ (V)	55.2	60
$V_{Lr}(t_1)$ (V)	83.0	110
V_{C1}(peak) (V)	85.9	90
$I_{Lr}(t_4)$ (A)	4.30	3.4
$V_{Lr}(t_4)$ (V)	-31.6	-38

Table 5.5 Comparisons of the Waveform Parameters

5.8 Power Loss Analysis

In order to further increase the efficiency of the resonant half bridge dual converter, the key power loss components have been identified. Both of the transformer open and short circuit experiments have been conducted to verify the designed loss values.

5.8.1 Power Loss Breakdown

The total power loss measured by the calorimetry method is 10.2W. In the experiment, the input power is 96W and the efficiency is 89.3%. The experimental data are recorded in Appendix 5. Table 5.6 shows the power loss breakdown in the

converter. From this table, we can see that the power loss in the mosfets is greatly reduced by eliminating the switching loss. However, this improvement is made at the cost of extra loss in additional resonant inductors and capacitors. The total estimated loss, 9.4W, compares very favorably with 10.2W loss measured by the calorimetry method.

Component	Estimated Power Loss (W)
Transformer T	3.7
Inductors L_1, L_2	1.2
Additional Resonant Inductor L_a	2.9
Mosfets Q_1, Q_2	0.4
Additional Resonant Capacitors C_{a1}, C_{a2}	0.4
Diodes D_1 to D_4	0.8
Total	9.4

Table 5.6 Power Loss Breakdown

Appendix 5 also indicates that the mosfet driving circuit for the resonant converter consumes a power of 2.46W. This is equivalent to 1.23W loss per mosfet and is high compared to the power consumption of the driving circuit for the hard-switched converter. However, a redesign by applying resonant technique to the gate driving circuit is expected to reduce this power losses.

The power losses in the transformer T, inductors L_1 and L_2 and additional resonant inductor L_a were estimated by measuring their temperature rise and calculating the

corresponding heat dissipation. The power losses in the mosfets, additional resonant capacitors and diodes are calculated according to their electrical specifications. The detailed calculation is shown in Appendix 6.

5.8.2 Transformer Open and Short Circuit Experiments

The actual power loss in the transformer is higher than the design value of 0.88W. The transformer current waveform is relatively clean and parasitic oscillation losses should be absent. In order to validate the total core and copper loss in the transformer, open and short circuit experiments were performed. Figures 5.18 and 5.19 respectively show the schematics of the two experiments.

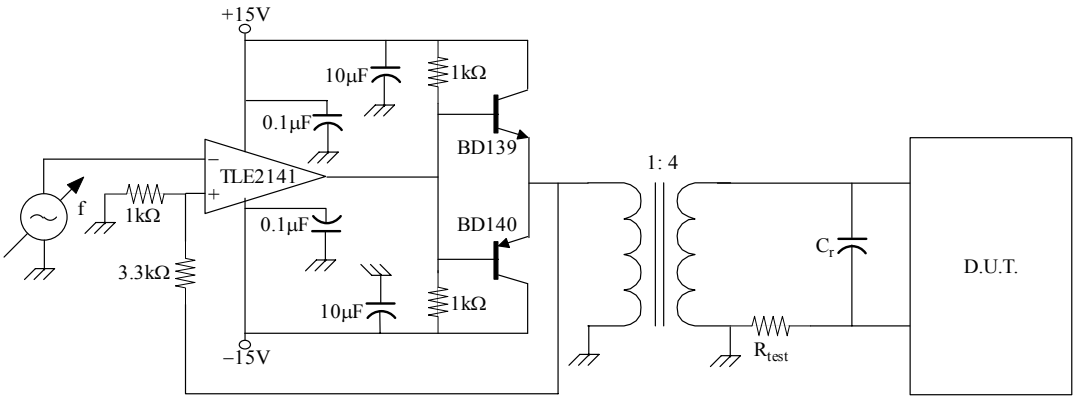


Figure 5.18 Open Circuit Experiment

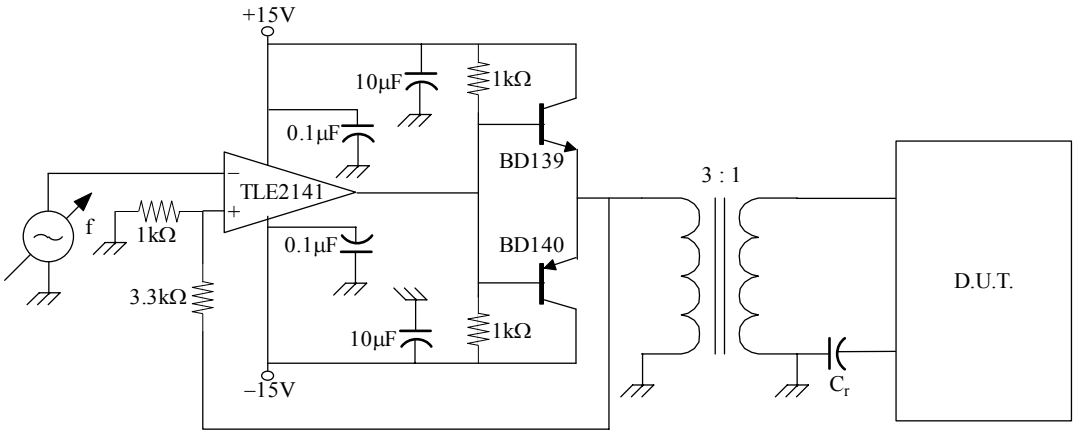


Figure 5.19 Short Circuit Experiment

Both experimental circuits utilize one operational amplifier, Texas Instrument TLE2141 and two power transistors, Philips BD139 of NPN type and BD140 of PNP type, to provide the excitation to the transformer under test. In the open circuit test, a step up transformer with the turns ratio of 1:4 is used to provide enough voltage input to the primary of the transformer under test and the transformer is gapped during the test to act as a self resonant transformer. In the short circuit test, a step down transformer with the turns ration of 3:1 is used to provide enough current input to the secondary of the transformer under test.

The open and short circuit experiments respectively established a copper loss of 0.7W and a core loss of 0.6W. The recorded data are given in Appendix 8. These results verified the total transformer copper and core loss is 1.3W and is not significantly higher than the design value.

The issue of additional transformer loss is not fully resolved. Given that the experimental waveforms are relatively clean, parasitic oscillations losses should not be an issue. Some possibilities include:

- Additional loss components due to harmonics given the non sinusoidal excitation.
- Losses due to dielectric loss in the insulation materials – capacitive elements elsewhere in the converter do have significant losses. A winding reversal time of 100ns implies a dv/dt of 7kV/μs in the transformer secondary.

The study of transformer loss has been complicated by the limitations of the experimental systems. The estimation of loss by observed temperature rise is inexact and it is difficult to recreate the circuit conditions in sinusoidal open and short circuit tests. It may take a significant amount of time to finally isolate the exact causes.

5.9 Improvements

The easiest way to increase the conversion efficiency is to optimize some major components in this converter. The optimizations are given in Table 5.7.

Component		Before Optimization	After Optimization
Transformer T	Core Type	Philips ETD29	Philips ETD34
	Ferrite Grade	Neosid F44	Philips 3F3
Additional Resonant Inductor L_a	Core Type	Philips ETD39 gapped	Philips ETD44 gapped
	Ferrite Grade	Philips 3C90	Philips 3F3
Additional Resonant Capacitors C_{a1}, C_{a2}	Type	Monolithic ceramic	Class COG surface mount
	Dissipation Factor	0.5%	0.1%
Mosfets Q_1, Q_2	Type Number	Intersil RFP40N10	ST STB50NE10
	Package	TO220	D^2PAK surface mount

Table 5.7 Components Optimizations

The new converter has an efficiency of 90.0%, measured by the calorimetry method. The total converter loss is established as 10.3W under the input power of 103W. Data are recorded in Appendix 5. Due to the usage of a better ferrite grade, Philips 3F3, the core loss of the new transformer is measured to be 0.3W, although the copper loss stays the same at 0.7W. The detailed experimental data are recorded in Appendix 8. The new resonant capacitors only have a dissipation factor of 0.1%, which is only one fifth of the dissipation factor of monolithic ceramic capacitors previously used. Under the same RMS current level, the power loss in the resonant capacitors is greatly reduced. Loss reduction also results from the resonant inductor, where a better ferrite grade is used and the introduction of surface mount mosfets and resonant capacitors, which helps in reducing the parasitic lead inductances.

5.10 Summary

This chapter discussed a soft-switched version of the half bridge dual converter. By actively using the parasitic components in the circuit, the operation frequency can be increased to four times of the operation frequency of the hard-switched converter and the converter efficiency reaches 90%. Under such a high operation frequency, the converter can be greatly reduced in both size and weight and is more suitable for MIC implementation in PV applications.

The converter was shown to have several operational modes which depend on load conditions and switch timing. An additional benefit of the topology is its tolerance to transformer capacitance. This allows soft switching to occur for the diodes and low loss rectification at 360V and 1MHz.

An extensive section on experimental results confirms the analysis presented for the converter. The experimental waveforms are very clean and generally the efficiencies and device losses are acceptable.

However, in order to maintain the resonance conditions against input voltage and load variations, the variable frequency control must be used, since the switching frequency is sensitive to the circuit parameters and the input and load conditions. A more desirable control technique is the constant frequency control, which achieves the PWM operation and can be realized by replacing the output rectifier diodes with active switches, [55]. Some other issues still remain with respect to additional

transformer losses. These issues along with the development of suitable control strategies are areas of future research.

6. CONCLUSIONS

With the sustained global shortage of conventional energy, more and more research work has been concentrated on the applications of PV energy. MIC technology has been recognized as a leading technology in grid interactive PV applications, which will become the mainstream of the worldwide PV market.

This thesis studies the development of the DC-DC converter, a key component in MIC implementations. A family of hard-switched and soft-switched half bridge dual converters, which are favorable for low voltage and high current photovoltaic inputs, has been developed. Theoretical analysis, simulation and experimental results are presented and it is concluded that the half bridge dual converter can be readily applied in MIC applications.

Considering the special requirements of a MIC in PV applications, the competing technology most available to date for the DC-DC conversion stage is the push-pull converter. However, it is stated that the push-pull converter has several disadvantages such as higher primary peak current, lower transformer copper utilization and the diode reverse recovery problem. Especially, under a wide range of input voltages, higher stresses exist in both of the main switches and rectifier diodes and this severely hinders its wide usage in MIC applications. The author firmly believes that the issue of output diode reverse recovery is so limiting in the push-pull converter that 1MHz operation at 360Vdc could not be easily achieved.

The disadvantages of the push-pull converter are successfully avoided by the half bridge dual converter. This can be verified by the experimental performance of the prototype hard-switched converter with an operating frequency of 100kHz. The efficiency of this prototype converter is 87.2%. However, the experimental results of the prototype converter do show one drawback of the new topology that the half bridge dual converter is sensitive to the level of the transformer leakage inductance.

In order to increase the operating frequency of the converter without sacrificing the efficiency, coaxial winding transformers are introduced in the hard-switched converter design. The new converter operates at 250kHz and takes the advantage of low leakage inductance of coaxial winding transformers to obtain 88.6% efficiency. The coaxial technique has been existing for years, but the idea to further reduce the leakage inductance through the transformer parallel arrangement in the matrix design is relatively new and places this converter on the cutting edge of the DC-DC converter design.

Although the circuits of hard-switched converters are relatively simple, limitations do exist for the operating frequency and the overall efficiency. Therefore, a soft-switched variation of the half bridge dual converter is developed. The soft-switched converter makes active use of circuit parasitic components such as transformer leakage inductance and switch output capacitance and reduces one significant part of power loss in hard-switched converters, the switching loss, to the greatest extent. By optimizing some circuit components, the converter finally reached an efficiency of 90%.

Considerable work has been done for all three converters in identifying the power loss components and improving the efficiencies by developing possible loss reduction schemes. However, this thesis does not completely resolve the issue related to the parasitic losses in the transformer. The author believes that its resolution requires more sophisticated tools and this presents a great challenge to the laboratory instrumentation. The use of the calorimetry method was critical in achieving the degree of loss resolution that was achieved. A final resolution of transformer loss may require a very detailed evaluation of the loss mechanisms and presents an opportunity for further research.

Other future work could include the study of resonant gate drive systems, integrated magnetics design, small signal modelling and the control technique development. The author will continue to work on the energy conversion technologies in the PV area and develop possible mechanisms to improve the overall performance of the converters suitable for MICs in PV applications.

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APPENDIX 1. BASIC BUCK AND BOOST DC-DC CONVERTERS

The underlying principles of DC-DC conversion can be explained by the elementary DC-DC converter shown in Figure A1.1(a). The switch S is operated with a switching period of T_s, where $T_s = t_{on} + t_{off}$, t_{on} is the duration when S is closed and t_{off} is the duration when S is open. The switching duty cycle, D, is defined as the ratio of the on time to the switching period

$$D = t_{on} / T_s = t_{on} f_s \tag{A1.1}$$

where $f_s = 1/T_s$ is the switching frequency.

Assuming that S is an ideal switch, that is, the switch conducts with zero voltage drop, blocks with zero leakage current and switches from one state to the other in zero time, the instantaneous output voltage v_o would be either the input voltage V_i or zero, as shown in Figure A1.1(b). The mean output voltage V_o can be obtained by averaging the integration of the instantaneous values of v_o in one complete switching period

$$V_o = \frac{1}{T_s}\int_0^{T_s} v_o(t)dt = \frac{1}{T_s}\int_0^{t_{on}} V_i dt = \frac{t_{on}}{T_s}V_i = DV_i \tag{A1.2}$$

However, the large proportion of ripple in the output voltage is normally not acceptable for most of the power supply applications and this can be filtered out by additional devices as included in buck converters.

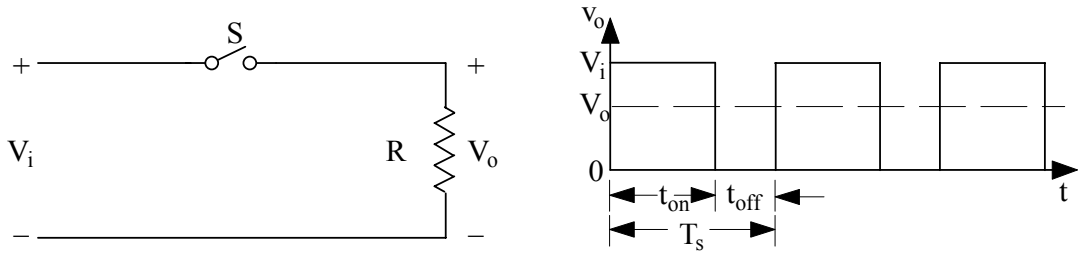


Figure A1.1 Elementary DC-DC Converter (a) Circuit (b) Output Voltage

A1.1 Basic Buck Converters

Figure A1.2 shows the elementary converter with a low-pass filter made up with an inductor and a capacitor. If S_1 is replaced with a semiconductor capable of interrupting forward current such as a mosfet and S_2 is replaced with a free-wheel diode, a basic buck converter can be formed. The circuit schematic of the buck converter and its equivalent circuits in different switching modes are respectively shown in Figures A1.3(a) and (b). The waveforms of this converter are illustrated in Figure A1.3(c).

The operation of the buck converter is the same as the elementary converter without the filter. When the mosfet S_1 is closed, the diode S_2 is reverse biased and the

inductor current linearly increase. When the mosfet S_1 is open, the diode S_2 conducts and the inductor current continues to fall.

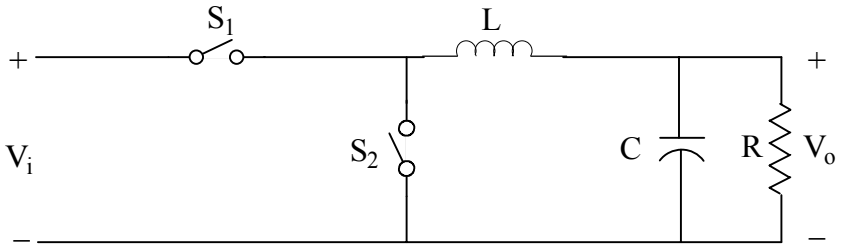
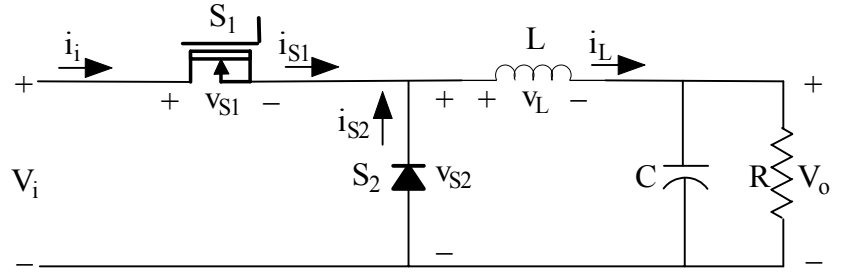
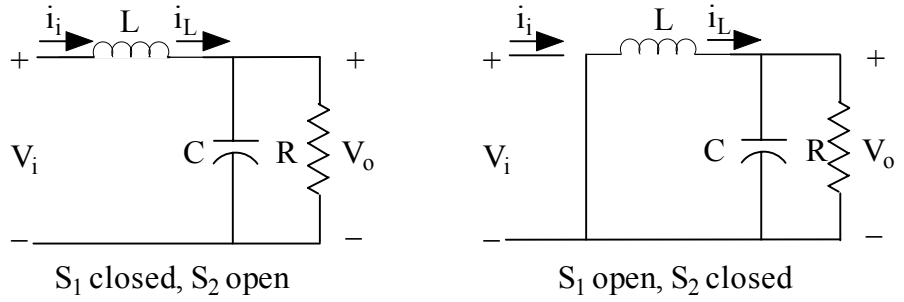


Figure A1.2 DC-DC Converter with a Low-Pass Filter

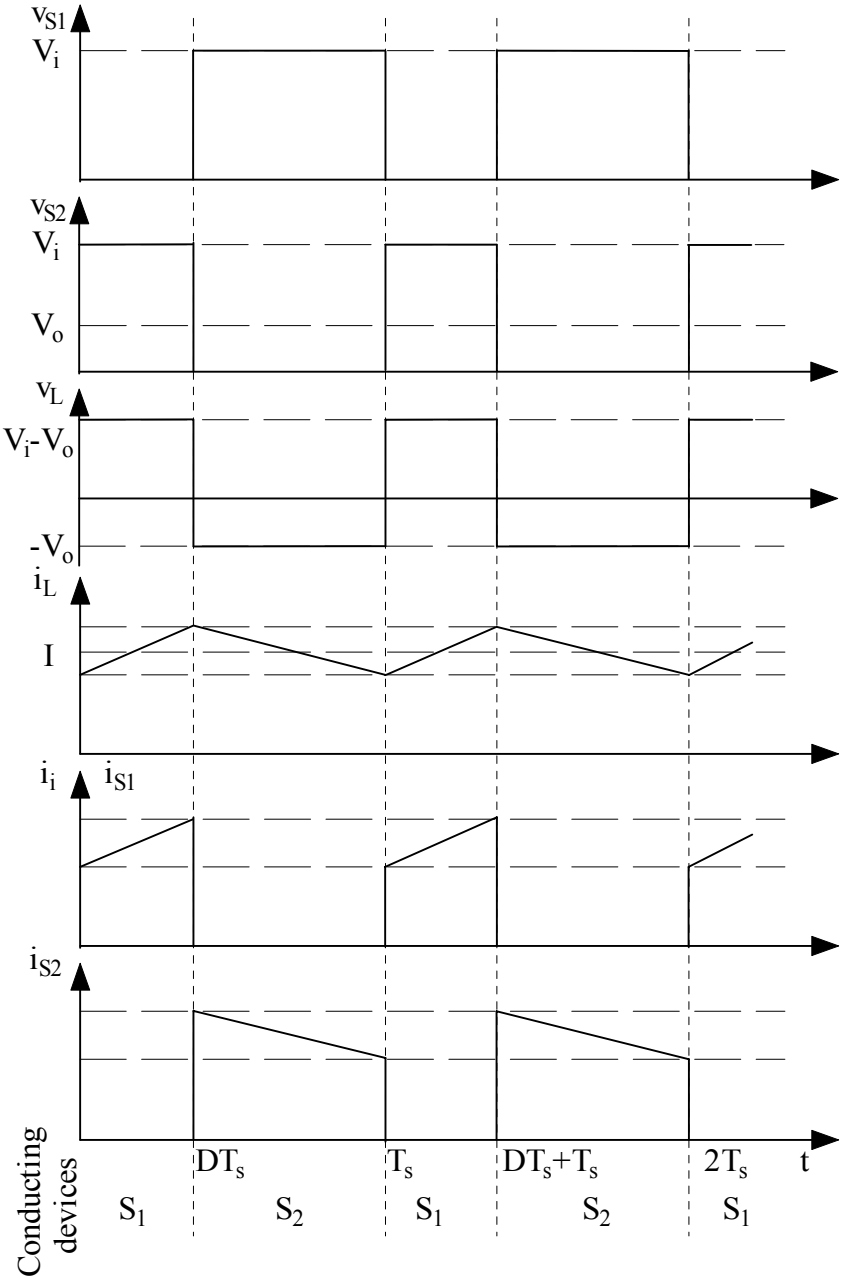


(a)



(b)

Figure A1.3 The Buck Converter (a) Schematic (b) Equivalent Circuits



(c)

Figure A1.3 The Buck Converter (Continued) (c) Waveforms

The dc output voltage can be calculated by taking the average of the integration of the output voltage in one complete switching period as discussed at the beginning of this appendix. However, a more standard calculation employs the principle of

inductor volt-second balance. In the steady state operation, the net change in inductor current over one switching period must be zero and therefore the inductor volt-seconds in one period must be added to zero. According to this principle,

$$(V_i - V_o)\cdot DT_s - V_o \cdot (T_s - DT_s) = 0 \tag{A1.3}$$

Rearranging the terms yields

$$V_o = DV_i \tag{A1.4}$$

This result is the same as Equation A1.2.

A1.2 Basic Boost Converters

In the buck converter, the output voltage is always smaller then the input voltage. In the case where the output voltage is required to be greater than the input voltage, a boost converter must be used. Figures 1.4(a) and (b) respectively show the circuit schematic of the basic boost converter and its equivalent circuits in different switching modes. The waveforms of this converter are given in Figure A1.4(c). The assumption of this analysis is that the output filter capacitor is large enough and no ripple exists in the output voltage.

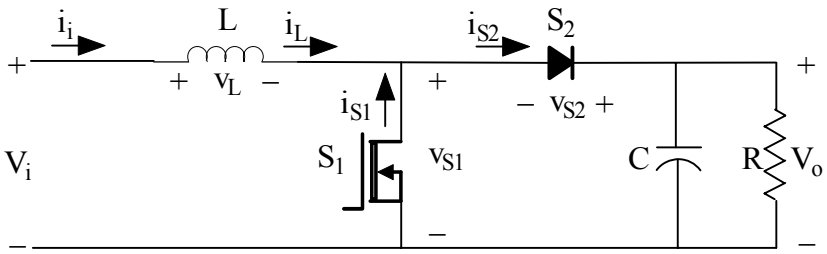
When the mosfet is closed, the diode is reverse biased and the inductor current ramps upward until the mosfet is open. At that time, the diode conducts and the inductor current linearly drops.

The output voltage can be calculated using the principle of inductor volt-second balance,

$$V_i \cdot DT_s + (V_i - V_o) \cdot (T_s - DT_s) = 0 \tag{A1.5}$$

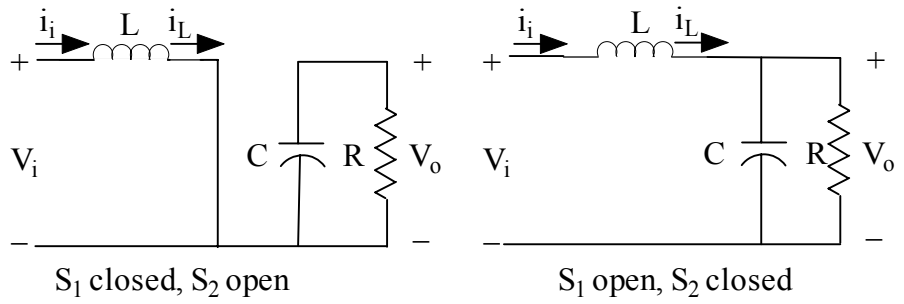
Rearranging the terms yields

$$V_o = \frac{1}{1-D} \cdot V_i \tag{A1.6}$$

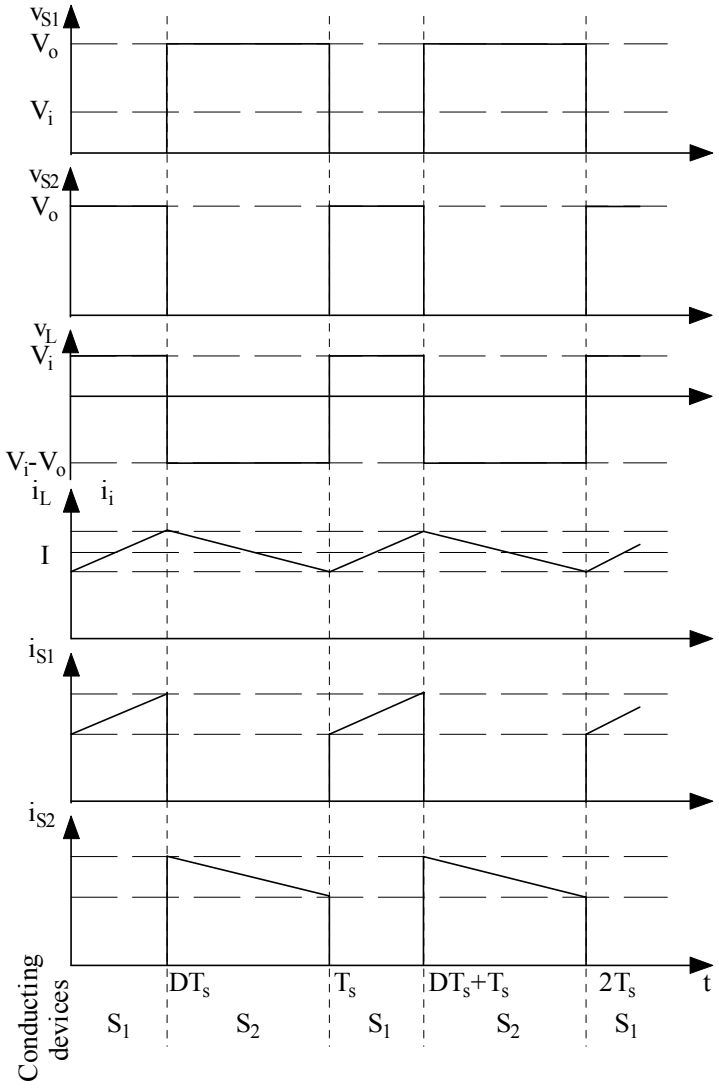


(a)

Figure A1.4 Basic Boost Converter (a) Schematic



(b)



(c)

Figure A1.4 Basic Boost Converter (Continued) (b) Equivalent Circuits (c) Waveforms

APPENDIX 2. THE CONDUCTION AND SWITCHING LOSSES IN SWITCHING SEMICONDUCTORS

For a switching semiconductor with R_{on} as its forward resistance, the conduction power loss is

$$P_{conduction} = I_{on}{}^2 R_{on} \tag{A2.1}$$

where I_{on} is the RMS current through the switching semiconductor. Equation A2.1 verifies that, for the same I_{on} value, the conduction loss in switching semiconductors is proportional to the on resistance R_{on}. However, this is not the case for the semiconductor switching loss. The switching power loss is proportional to the switching frequency. Simplified current and voltage waveforms in switching semiconductors during turn on and turn off are given in Figure A2.1. The energy dissipated in the semiconductor during turn-on is

$$W_{on} = \int_0^{t_r} v(t)i(t)dt = \int_0^{t_r} EI\frac{t}{t_r}dt = \frac{1}{2}EIt_r \tag{A2.2}$$

The energy dissipated in the semiconductor during turn-off is

$$W_{off} = \int_0^{t_f} v(t)i(t)dt = \int_0^{t_f} EI\frac{t_f - t}{t_f}dt = \frac{1}{2}EIt_f \tag{A2.3}$$

Therefore, the switching power loss can be calculated to be

$$P_{switching} = \frac{W_{on} + W_{off}}{T_s} = \frac{1}{T_s}\left(\frac{1}{2}EIt_r + \frac{1}{2}EIt_f\right) = \frac{1}{2}f_s EI\left(t_r + t_f\right) \qquad \text{(A2.4)}$$

where $f_s = 1/T_s$ is the switching frequency.

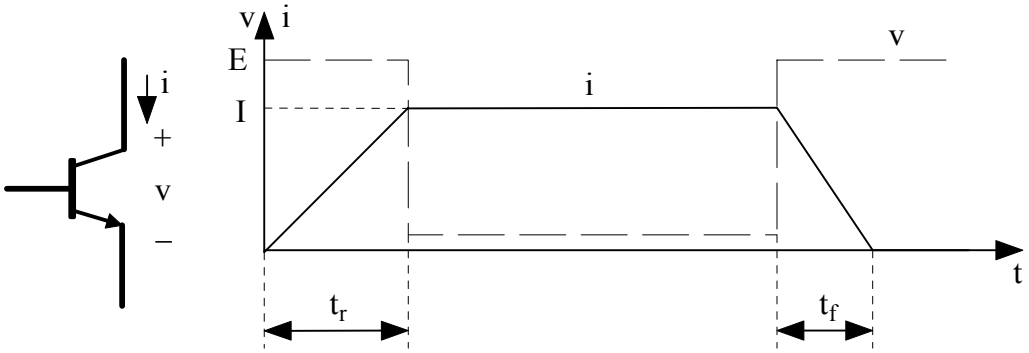


Figure A2.1 Simplified Turn On and Turn Off Waveforms in the Switching Semiconductor

APPENDIX 3. SNUBBER CIRCUITS

Snubber circuits are very helpful in reducing the electrical stresses of the power semiconductor devices in the electronic converters. Different types of snubber circuits are used under different requirements. This appendix mainly concentrates on two types of snubber circuits: the turn-on snubber and the turn-off snubber, which are often found in DC-DC converters.

A3.1 Turn-On Snubber

The circuit of a typical turn-on snubber is shown in Figure A3.1. The snubber is made up of an inductor L_s, a diode D_{Ls} and a resistor R_{Ls}. Before the mosfet Q turns on, the load current I flows in the freewheeling diode D. At turn on, the load current starts to divert to the inductor L_s and the mosfet drain and the current in the diode D decreases. Assuming that the current in the inductor L_s increases linearly, there will be a steady voltage drop across L_s and the mosfet drain source voltage during turn on is reduced. The voltage and current waveforms with and without the turn-on snubber during turn on are given in Figure A3.2.

During the on-state of the mosfet, L_s conducts I and the energy stored in L_s is $L_s I^2 / 2$. This energy will dissipate in the snubber resistor R_{Ls} when the mosfet Q turns off.

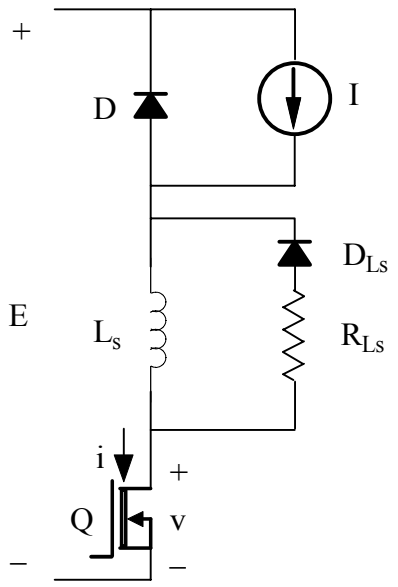


Figure A3.1 Turn-On Snubber

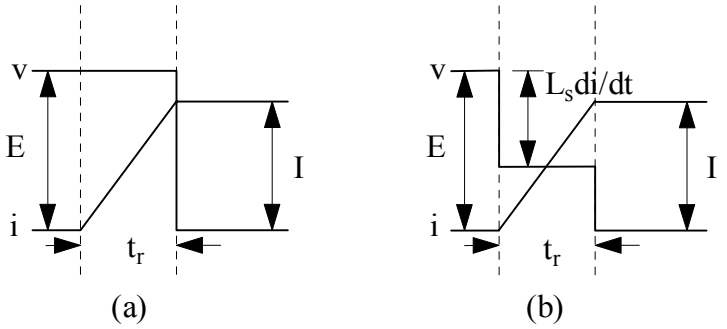


Figure A3.2 Voltage and Current Waveforms (a) without Snubber (b) with Snubber

A3.2 Turn-Off Snubber

The turn-off snubber circuit is shown in Figure A3.3. The turn-off snubber consists of a capacitor C_s, a diode D_{Cs} and a resistor R_{Cs}. Prior to the turn off of the mosfet Q, it conducts the load current I. When Q begins to turn off, the mosfet drain current linearly decreases and the difference between the load and drain current

flows into the snubber capacitor C_s because the diode D will stay reverse biased unless the mosfet drain source voltage reaches E. The voltage and current waveforms with and without the turn-off snubber during turn off are shown in Figure A3.4.

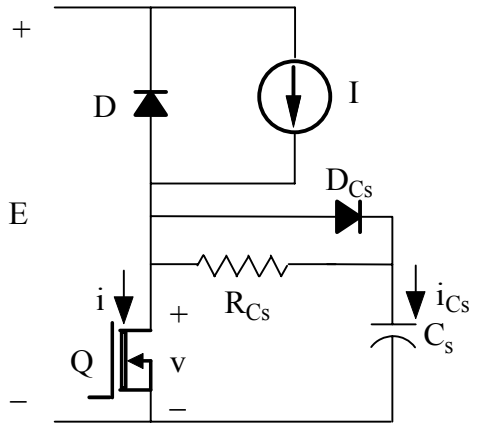


Figure A3.3 Turn-Off Snubber

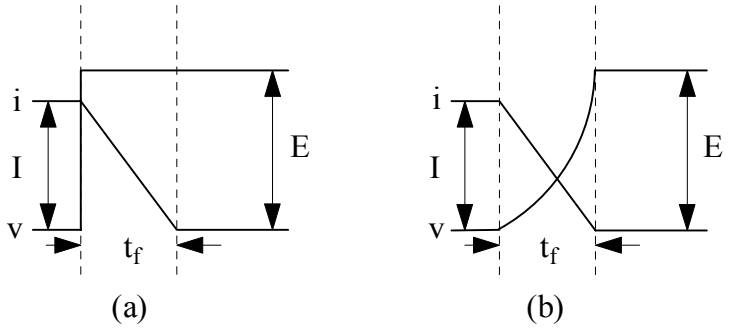


Figure A3.4 Voltage and Current Waveforms (a) without Snubber (b) with Snubber

Under the assumption that the mosfet drain current linearly decreases, i and i_{Cs} during turn off period can be written as

$$i = I - I \cdot t / t_f \tag{A3.1}$$

$$i_{Cs} = I - i = I \cdot t / t_f \tag{A3.2}$$

The capacitor voltage is

$$v_{Cs} = \frac{1}{C_s} \int_0^t i_{Cs} dt = \frac{I}{2C_s t_f} t^2 \tag{A3.3}$$

During the off-state of the mosfet, C_s supports E and the energy stored in C_s is $C_s E^2 / 2$. This energy will dissipate in the snubber resistor R_{Ls} when the mosfet Q turns on.

APPENDIX 4. CONVERTER DESIGN PROCESS

Main components in the half bridge dual converter include Transformer T, Inductors L_1 and L_2, Mosfets Q_1 and Q_2, Diodes D_1 to D_4 and Capacitor C_o. The design processes of these components are similar in both of the hard-switched and the soft-switched converters. Because the duty cycle of each switch in the experiment is only slightly higher than 50%, the design may be simplified if it is based on 50% switch duty cycle. The detailed design process of the main components in the prototype converter stated in Section 4.1 of Chapter four is listed below as an example.

A4.1 Transformer

The design and calculation in this section use some data including soft ferrite material grade specifications and core parameters from *Philips Data Handbook MA01: Soft Ferrite*, released on August 30, 1995. The page numbers where the reference data or figures are located will be given in brackets.

The transformer excitation frequency of the prototype converter is 50kHz. The waveforms of the transformer input and output voltages and the flux density under 50% duty cycle are given in Figure A4.1. The transformer design steps are as the following.

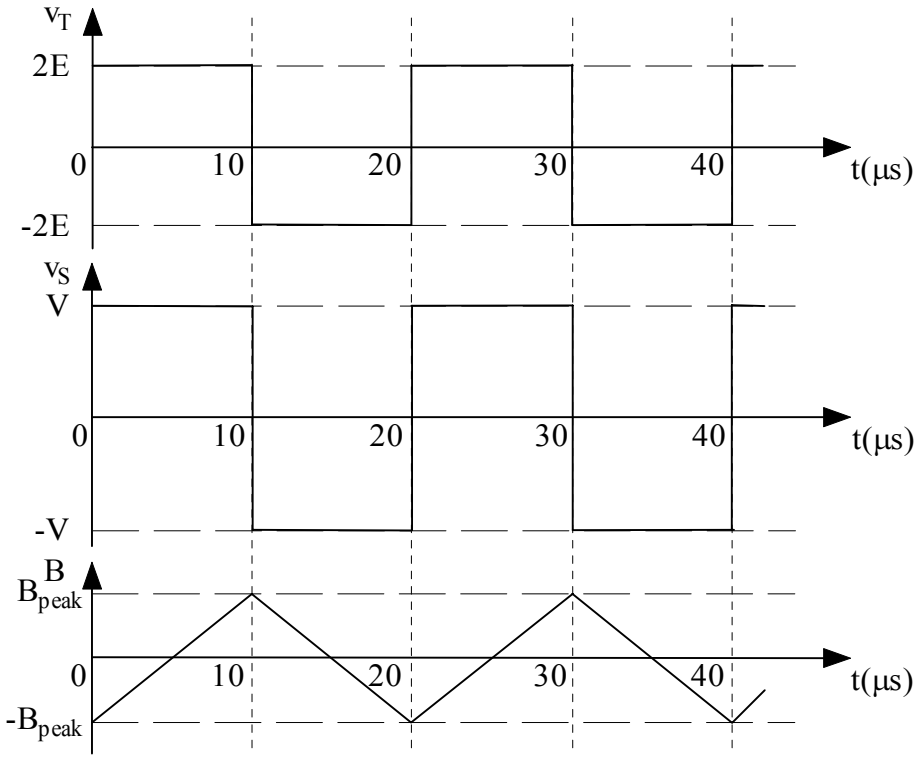


Figure A4.1 Transformer Voltage and Flux Density Waveforms

1. Core loss and copper loss (P_{core} and P_{Cu})

   Transformer power rating $P = 88W$;

   Set the transformer efficiency $\eta = 99\%$;

   Total power loss for the transformer $P_{loss} = P \cdot (1-\eta) = 0.88W$;

   Core loss $P_{core} = \frac{1}{2} P_{loss} = 0.44W$;

   Copper loss $P_{Cu} = \frac{1}{2} P_{loss} = 0.44W$;

   Primary copper loss $P_p = \frac{1}{2} P_{Cu} = 0.22W$;

   Secondary copper loss $P_s = \frac{1}{2} P_{Cu} = 0.22W$.

2. Total change of flux density (ΔB)

   Core set effective volume $V_e = 10800mm^3$ (Page 298);

   Transformer core loss density $P_v = \frac{P_{core}}{V_e} = 41kW/m^3$;

   Peak flux density $B_{peak} = 80mT$ (Figure 6, Page 95);

   Total change of flux density $\Delta B = 2B_{peak} = 160mT$.

3. Primary and secondary number of turns (N_p and N_s)

   Core minimum area $A_{\min} = 106mm^2$ (Page 298);

   Linkage change per turn $\Delta\lambda = \Delta B \cdot A_{\min} = 16.96\mu Wb = 16.96V \cdot \mu s$;

   Switching frequency $f_s = 50kHz$;

   Switching period $T_s = 1/f_s = 20\mu s$;

   Voltage per turn $V_{turn} = \frac{\Delta\lambda}{T_s/2} = 1.696V$;

   Input voltage $E = 17.6V$;

   Primary number of turns $N_p = \frac{2E}{V_{turn}} = 20.8 = 21turns$;

   Output voltage $V = 360V$;

   Secondary number of turns $N_s = \frac{V}{V_{turn}} = 212.3 = 212turns$;

   Check the actual maximum total change of flux density

   $$(\Delta B)_{actual,\max} = \frac{V(T_s/2)}{N_s A_{\min}} = 160.2mT.$$

4. Primary and secondary conductor diameter (d_p and d_s)

   Average length of turn $l_{turn} = 62.4mm$ (Page 300);

   Input current $I_s = 5A$;

   Transformer primary RMS current $I_p = \frac{I_s}{2} = 2.5A$;

   Primary winding conductor dc resistance $R_p = \frac{P_p}{I_p^2} = 0.0352\Omega$;

   Primary winding conductor cross section area $A_p = \frac{\rho N_p l_{turn}}{R_p} = 0.640mm^2$;

   Primary conductor diameter $d_p = 2\sqrt{\frac{A_p}{\pi}} = 0.90mm$;

   Secondary conductor diameter $d_s = d_p\sqrt{\frac{N_p}{N_s}} = 0.28mm$.

   The actual conductors selected for the transformer windings are listed in Table A4.1.

Winding Conductor	Copper Diameter (mm)	Overall Diameter (mm)	DC Resistance (Ω)
Primary	1.00	1.06	0.0287
Secondary	0.32	0.36	2.83

Table A4.1 Transformer Winding Conductors

5. Winding allocations in the transformer core former

   The secondary winding can be fit into the core former in four layers and the primary winding forms one layer, sandwiched between the secondary winding,

as shown in Figure A4.2. The shaded areas are the insulation between the primary and the secondary windings.

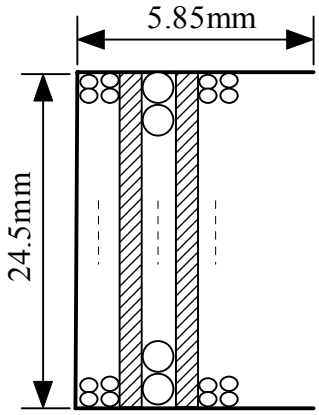


Figure A4.2 Winding Allocations in the Core Former

6. Leakage inductance referred to the primary side ($L_{leakage}$)

Primary number of turns $N_p = 21 turns$;

The number of section interfaces $M = 2$;

Average length of turn $l_{turn} = 62.4mm$;

The winding dimension parallel to the section interfaces $Y = 24.5mm$;

The sum of all section dimensions perpendicular to the section interfaces

$\Sigma x = 1.06mm + 0.36mm \times 4 = 2.5mm$;

The sum of all intersection layer thicknesses $\Sigma x_{\Delta} = 0.6mm \times 2 = 1.2mm$;

Leakage inductance referred to the primary side [23]

$$L_{leakage} = 4\pi \cdot 10^{-4} \frac{N_p^2 l_{turn}}{M^2 Y} \left(\frac{\Sigma x}{3} + \Sigma x_{\Delta} \right) = 0.72 \mu H .$$

7. Magnetising inductance referred to the primary side (L_m)

   Core inductance factor $A_L = 2700nH$ (Page 298);

   Primary number of turns $N_p = 21turns$;

   Magnetising inductance referred to the primary side $L_m = N_p^2 \cdot A_L = 1.19mH$.

8. Primary and secondary resistance factor (F_{Rp} and F_{Rs})

   - Primary resistance factor (F_{Rp})

     Primary number of turns $N_p = 21turns$;

     Total number of layers in the complete primary winding $N_{layer,p} = 1$;

     The number of primary turns per layer $N_{l,p} = \dfrac{N_p}{N_{layer,p}} = 21turns$;

     Primary conductor diameter $d_p = 1.00mm$;

     Effective primary conductor breadth $b_p = 0.886d_p = 0.886mm$;

     The overall winding breadth $b_w = 24.5mm$;

     The primary layer copper factor $F_{l,p} = \dfrac{N_{l,p} b_p}{b_w} = 0.759$;

     The penetration depth at 50kHz $\Delta = 72mm \cdot Hz^{1/2} \cdot f_s^{-1/2} = 0.322mm$;

     The effective primary conductor height $h_p = 0.886d_p / 2 = 0.443mm$;

     The primary ac resistance parameter $\varphi_p = \dfrac{h_p \sqrt{F_{l,p}}}{\Delta} = 1.20$;

     The number of layers in each primary winding portion $p_p = 1/2$;

     According to Figure A4.3, the primary resistance factor $F_{Rp} = 1.0$.

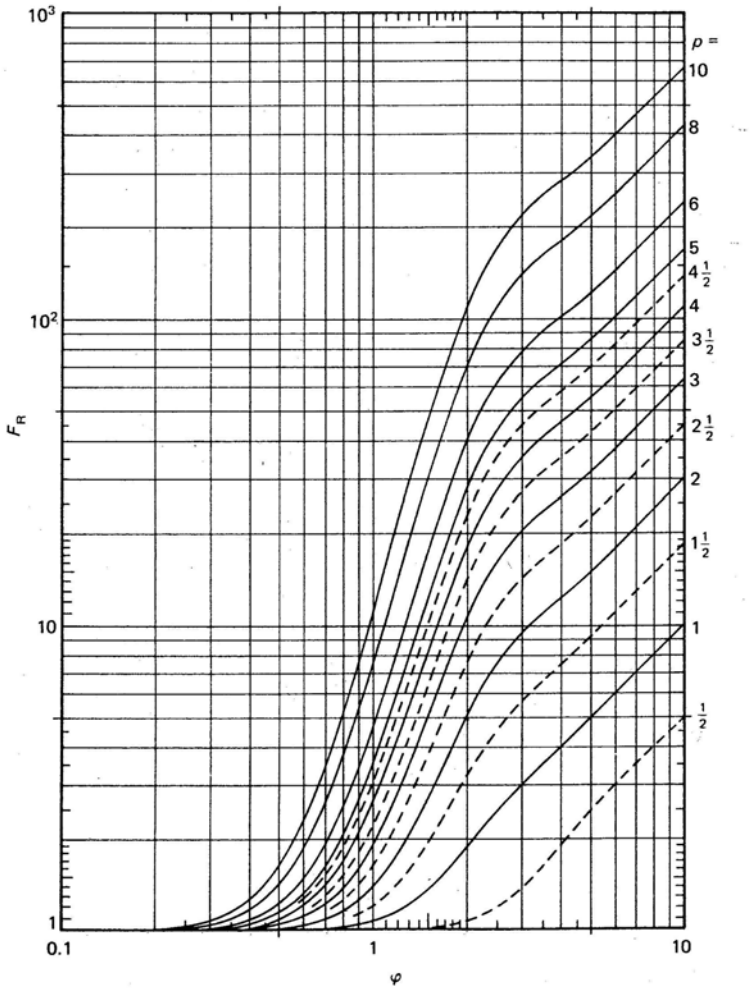


Figure A4.3 Resistance Factor as a Function of φ and p

(Reproduced from Figure 11.14 on page 329 of reference [27])

- Secondary resistance factor (F_{Rs})

  Secondary number of turns $N_s = 212 turns$;

  Total number of layers the complete secondary winding $N_{layer,s} = 4$;

  The number of secondary turns per layer $N_{l,s} = \frac{N_s}{N_{layer,s}} = 53 turns$;

  Secondary conductor diameter $d_s = 0.32 mm$;

Effective secondary conductor breadth $b_s = 0.886 d_s = 0.284 mm$;

The secondary layer copper factor $F_{l,s} = \frac{N_{l,s} b_s}{b_w} = 0.614$;

The effective secondary conductor height $h_s = 0.886 d_s = 0.284 mm$;

The secondary ac resistance parameter $\varphi_s = \frac{h_s \sqrt{F_{l,s}}}{\Delta} = 0.69$;

The number of layers in each secondary winding portion $p = 2$;

According to Figure A4.3, the secondary resistance factor $F_R = 1.1$.

A4.2 Inductor

Average inductor current $I_L = 2.5A$;

Set maximum change of inductor current $\Delta I_L = 1A$;

Inductance $L_1 = L_2 = \frac{E \cdot T_s / 2}{\Delta I_L} = 176 \mu H$;

Core inductance factor $A_L = 250 nH$;

Number of turns $N_L = \sqrt{\frac{L_1}{A_L}} = 26.5 = 27 turns$.

A4.3 Mosfet

Maximum drain source voltage $V_{DS,\max} = 2E = 35.2V$;

Maximum drain current $I_{D,\max} = 5A$;

A4.4 Diode

Maximum reverse voltage $V_{R,\max} = V = 360V$;

Maximum forward current $I_{F,\max} = P/V = 0.24A$.

A4.5 Capacitor

Set maximum change of capacitor voltage $\Delta V = 2.5V$;

Load current $I = P/V = 0.24A$;

Capacitance $C_o = \dfrac{I \cdot T_s / 2}{\Delta V} = 0.96\mu F = 1\mu F$.

APPENDIX 5. CALORIMETRY METHOD

For an efficient converter, the determination of loss is extremely difficult from input/output measurements. When measuring the power loss of high frequency DC-DC converters, most digital instruments will misbehave due to the high frequency components in the converter input and/or output and accurate results cannot be obtained. Calorimetry method provides an indirect power loss measurement method and it can obtain more accurate measurement. The measurement must be conducted in a closed insulated container, such as a beer cooler. Other devices installed inside the container include:

- A fan, which is used to stir the air inside so that no hot spot exists,
- Several temperature sensors, such as National Semiconductor LM35, which are used to measure the temperatures of different spots inside,
- The device under test, which is the DC-DC converter in this case, and
- A power resistor with the power rating of at least the estimated total loss of the device under test.

At least one temperature sensor has to be installed outside to measure the ambient temperature. The container must be sealed before the experiment is carried out. The experiment proceeds in two stages: the system calibration stage and the power loss measurement stage.

In the system calibration stage, different input voltages are applied to the power resistor. Data of the stabilized temperature rise against the power input are recorded and a linear graph, a straight line for the two variables, can be obtained.

The next stage is the actual power loss measurement. In this stage, the system has to be kept unchanged and the voltage source is applied at the converter under test. When the whole system reaches its thermal equilibrium, the temperature rise is recorded. By comparing this temperature rise with the calibration graph, the total power loss of the converter can be easily obtained.

The experimental data recorded for each converter are given in the following sections. The efficiencies calculated here are the efficiencies of the converter main circuit and only related to the input and output powers of the main circuit. Therefore, the power dissipation of the driving circuit must be subtracted from the total power loss measured by the calorimetry method.

A5.1 Data Recorded for the Prototype Converter

The data recorded for the system calibration are listed in Table A5.1. The calibration graph is shown in Figure A5.1. The recorded data for the converter are listed in Table A5.2.

The calculation of the power loss and the efficiency is given below.

The converter input power $P_{converter} = 17.94V \times 4.83A = 86.65W$;

The driver input power $P_{driver} = 12.22V \times 0.027A = 0.33W$;

System temperature rise $\Delta T = 35.4°C - 23.4°C = 12.0°C$;

Total power loss $P_{loss} = \frac{\Delta T - 1.503}{0.9223} = 11.38W$;

Efficiency $\eta = \left(1 - \frac{P_{loss} - P_{driver}}{P_{converter}}\right) \times 100\% = 87.2\%$.

Input Voltage (V)	Input Current (A)	Input Power (W)	Ambient Temperature (ºC)	System Temperature (ºC)	Temperature Rise (ºC)
3.16	0.31	0.98	21.5	24.2	2.7
4.48	0.44	1.97	23.3	26.5	3.2
5.48	0.54	2.96	21.7	25.8	4.1
6.20	0.61	3.78	21.5	26.6	5.1
7.07	0.70	4.95	22.3	28.1	5.8
7.55	0.74	5.59	23.3	29.6	6.3
8.36	0.82	6.86	23.3	31.4	8.1
9.06	0.89	8.06	24.7	34.0	9.3
9.75	0.96	9.36	22.7	32.9	10.2
10.01	0.98	9.81	24.9	35.2	10.3
10.81	1.06	11.46	24.3	36.4	12.1

Table A5.1 Calibration Data

Converter Input Voltage (V)	Converter Input Current (A)	Driver Input Voltage (V)	Driver Input Current (A)	Room Ambient Temperature (ºC)	System Equilibrium Temperature (ºC)
17.94	4.83	12.22	0.027	23.4	35.4

Table A5.2 Recorded Data for the Prototype Converter

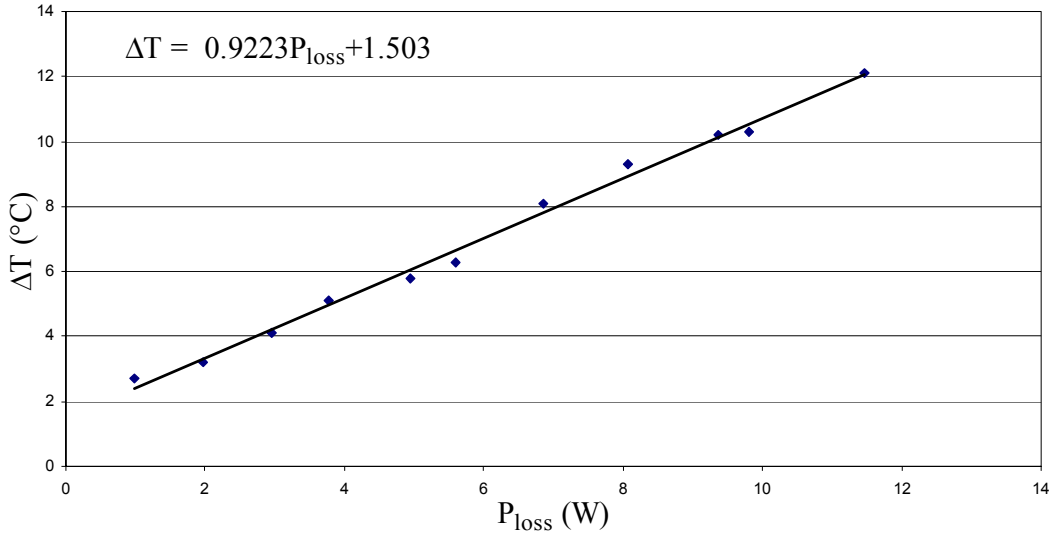


Figure A5.1 Calibration Graph

A5.2 Data Recorded for the Converter with a Coaxial Matrix Transformer

The data recorded for the system calibration are listed in Table A5.3. The calibration graph is shown in Figure A5.2. The recorded data for the converter are listed in Table A5.4.

The calculation of the power loss and the efficiency is given below.

The converter input power $P_{converter} = 16.38V \times 5.48A = 89.76W$;

The driver input power $P_{driver} = 12.01V \times 0.0401A = 0.48W$;

System temperature rise $\Delta T = 36.1°C - 24.6°C = 11.5°C$;

Total power loss $P_{loss} = \frac{\Delta T - 1.562}{0.9283} = 10.71W$;

Efficiency $\eta = \left(1 - \frac{P_{loss} - P_{driver}}{P_{converter}}\right) \times 100\% = 88.6\%$.

Input Voltage (V)	Input Current (A)	Input Power (W)	Ambient Temperature (ºC)	System Temperature (ºC)	Temperature Rise (ºC)
3.45	0.34	1.17	23.5	26.3	2.8
4.50	0.44	1.98	24.0	27.5	3.5
5.59	0.55	3.07	23.2	27.6	4.4
6.47	0.65	4.21	23.7	28.9	5.2
7.04	0.69	4.86	25.6	31.3	5.7
7.80	0.77	6.01	22.4	30.0	7.6
8.52	0.84	7.16	25.1	33.2	8.1
8.99	0.89	8.00	25.4	34.3	8.9
9.50	0.93	8.84	25.4	35.0	9.6
10.10	0.99	10.00	24.2	35.4	11.2
10.77	1.06	11.42	25.3	37.6	12.3
11.20	1.10	12.32	23.0	35.8	12.8

Table A5.3 Calibration Data

Converter Input Voltage (V)	Converter Input Current (A)	Driver Input Voltage (V)	Driver Input Current (A)	Room Ambient Temperature (ºC)	System Equilibrium Temperature (ºC)
16.38	5.48	12.01	0.0401	24.6	36.1

Table A5.4 Recorded Data for the Converter with a Coaxial Matrix Transformer

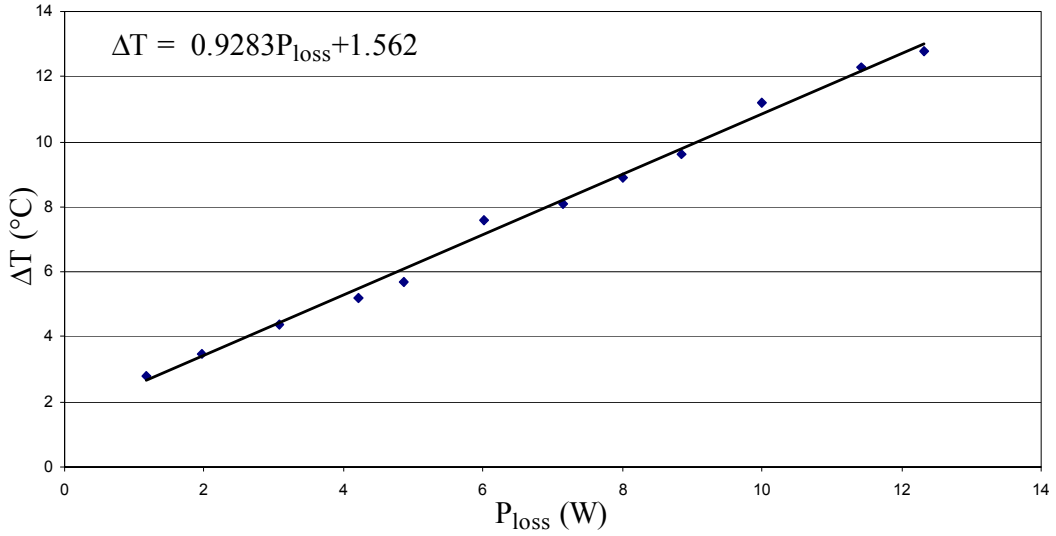


Figure A5.2 Calibration Graph

A5.3 Data Recorded for the Resonant Converter

The data recorded for the system calibration are listed in Table A5.5. The calibration graph is shown in Figure A5.3. The recorded data for the converter are listed in Table A5.6.

The calculation of the power loss and the efficiency is given below.

The converter input power $P_{converter} = 20.42V \times 4.70A = 95.97W$;

The driver input power $P_{driver} = 14.99V \times 0.164A = 2.46W$;

System temperature rise $\Delta T = 40.0°C - 27.0°C = 13.0°C$;

Total power loss $P_{loss} = \frac{\Delta T - 1.1967}{0.9302} = 12.69W$;

Efficiency $\eta = \left(1 - \frac{P_{loss} - P_{driver}}{P_{converter}}\right) \times 100\% = 89.3\%$.

Input Voltage (V)	Input Current (A)	Input Power (W)	Ambient Temperature (ºC)	System Temperature (ºC)	Temperature Rise (ºC)
3.42	0.34	1.16	26.1	28.1	2.0
4.64	0.46	2.13	26.1	29.2	3.1
5.72	0.56	3.20	26.3	30.5	4.2
6.77	0.67	4.54	26.2	31.8	5.6
7.29	0.72	5.25	26.4	32.5	6.1
7.83	0.77	6.03	26.1	33.2	7.1
8.54	0.84	7.17	26.4	34.3	7.9
9.09	0.90	8.18	26.3	35.1	8.8
9.74	0.96	9.35	26.3	36.3	10.0
10.06	0.99	9.96	26.5	37.0	10.5
10.63	1.05	11.16	26.0	37.4	11.4
11.10	1.09	12.10	26.4	38.7	12.3

Table A5.5 Calibration Data

Converter Input Voltage (V)	Converter Input Current (A)	Driver Input Voltage (V)	Driver Input Current (A)	Room Ambient Temperature (ºC)	System Equilibrium Temperature (ºC)
20.42	4.70	14.99	0.164	27.0	40.0

Table A5.6 Recorded Data for the Resonant Converter

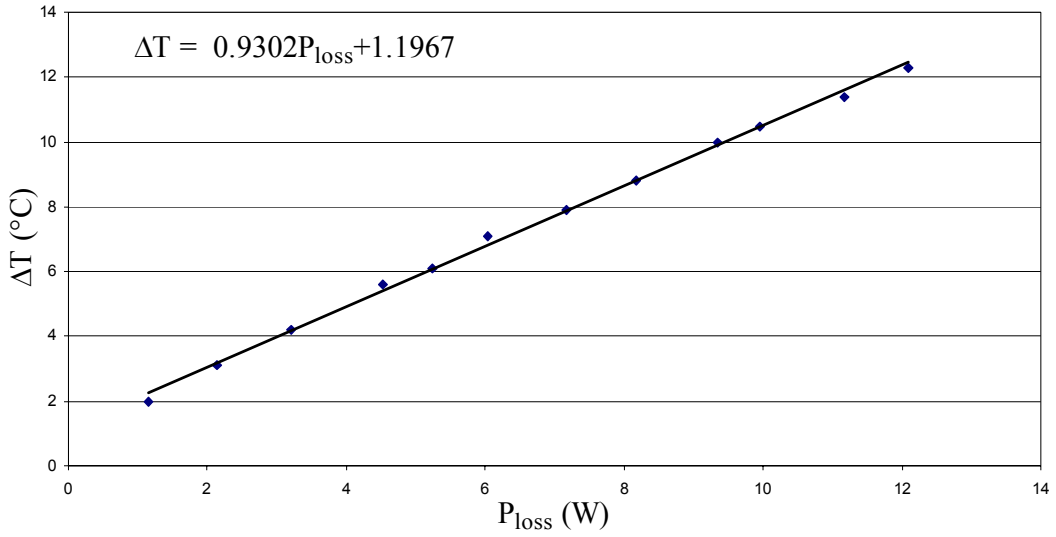


Figure A5.3 Calibration Graph

A5.4 Data Recorded for the Resonant Converter with Optimized Components

The data recorded for the system calibration are listed in Table A5.7. The calibration graph is shown in Figure A5.4. The recorded data for the converter are listed in Table A5.8.

The calculation of the power loss and the efficiency is given below.

The converter input power $P_{converter} = 23.88V \times 4.32A = 103.16W$;

The driver input power $P_{driver} = 15.09V \times 0.231A = 3.49W$;

System temperature rise $\Delta T = 40.0°C - 25.9°C = 14.1°C$;

Total power loss $P_{loss} = \frac{\Delta T - 0.6174}{0.9741} = 13.84W$;

Efficiency $\eta = \left(1 - \frac{P_{loss} - P_{driver}}{P_{converter}}\right) \times 100\% = 90.0\%$.

Input Voltage (V)	Input Current (A)	Input Power (W)	Ambient Temperature (ºC)	System Temperature (ºC)	Temperature Rise (ºC)
3.19	0.31	0.99	23.6	25.0	1.4
4.54	0.45	2.04	23.7	26.2	2.5
5.55	0.55	3.05	23.8	27.5	3.7
6.34	0.63	3.99	24.3	28.9	4.6
7.14	0.70	5.00	24.8	30.6	5.8
7.85	0.77	6.04	24.6	31.0	6.4
8.45	0.83	7.01	25.9	33.4	7.5
9.03	0.89	8.04	22.5	30.6	8.1
9.59	0.94	9.01	23.6	33.4	9.8
10.16	1.00	10.16	24.4	34.7	10.3
10.58	1.04	11.00	24.3	35.7	11.4
11.08	1.09	12.08	24.8	37.1	12.3

Table A5.7 Calibration Data

Converter Input Voltage (V)	Converter Input Current (A)	Driver Input Voltage (V)	Driver Input Current (A)	Room Ambient Temperature (ºC)	System Equilibrium Temperature (ºC)
23.88	4.32	15.09	0.231	25.9	40.0

Table A5.8 Recorded Data for the Resonant Converter with Optimized Components

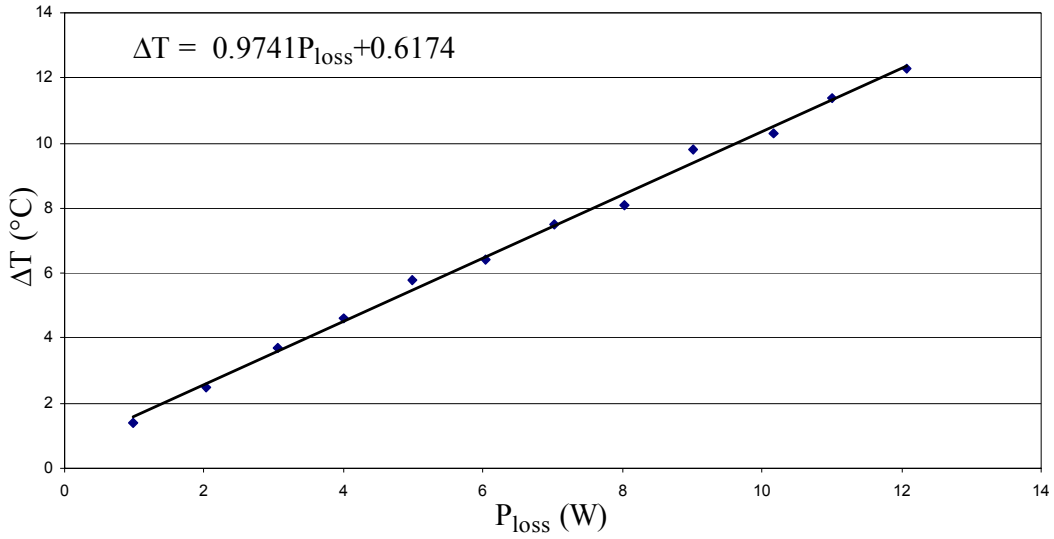


Figure A5.4 Calibration Graph

APPENDIX 6. POWER LOSS BREAKDOWN ANALYSIS

Power losses of the key components in the converter are estimated by either observing the stabilized temperature rise of the device so as to obtain the power loss indirectly or calculating the power loss directly according to the device electrical specifications. The detailed calculation is given below.

A6.1 Power Loss Breakdown for the Prototype Converter

The recorded equilibrium temperatures of the key components in the converter are listed in Table A6.1.

Temperature	Room	Transformer	Inductor	Mosfet	Zener	Diode
T_C (ºC)	23	52	41	44	83	30
T_K (K)	296	325	314	317	356	303

Table A6.1 Equilibrium Temperatures

1. Transformer

   (a) Rate of heat dissipation by radiation (P_{rad})

   Emissivity of the transformer surface $E = 0.95$;

   Rate of heat dissipation by radiation

   $$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T^4_{transformer,K} - T^4_{room,K}\right) = 187.5 W/m^2 .$$

   (b) Rate of heat dissipation by convection (P_{conv})

Temperature rise of the transformer $\theta = T_{transformer,K} - T_{room,K} = 29K$;

Horizontal dimension of the transformer $d_{hor} = 41.6mm$;

Vertical dimension of the transformer $d_{vert} = 39.0mm$;

Effective dimension of the transformer $d = \frac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 20.1mm$;

Rate of heat dissipation by convection $P_{conv} = 6.3\frac{\theta^{1.25}}{d^{0.25}} = 200.2W/m^2$.

(c) Total power loss in the transformer ($P_{transformer}$)

Total transformer surface area

$$A_s = 4 \times 41.6mm \times 39.0mm + 2 \times (41.6mm)^2 = 1 \times 10^{-2} m^2;$$

Total power loss in the transformer $P_{transformer} = (P_{rad} + P_{conv})A_s = 3.9W$.

2. Inductor

(a) Rate of heat dissipation by radiation (P_{rad})

Emissivity of the inductor surface $E = 0.95$;

Rate of heat dissipation by radiation

$$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T^4_{inductor,K} - T^4_{room,K}\right) = 110.1W/m^2 .$$

(b) Rate of heat dissipation by convection (P_{conv})

Temperature rise of the inductor $\theta = T_{inductor,K} - T_{room,K} = 18K$;

Horizontal dimension of the inductor $d_{hor} = 34.8mm$;

Vertical dimension of the inductor $d_{vert} = 29.0mm$;

Effective dimension of the inductor $d = \frac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 15.8mm$;

Rate of heat dissipation by convection $P_{conv} = 6.3\frac{\theta^{1.25}}{d^{0.25}} = 117.2W/m^2$.

(c) Total power loss in the inductors ($P_{inductor}$)

Total inductor surface area

$$A_s = 4 \times 34.8mm \times 29.0mm + 2 \times (34.8mm)^2 = 7 \times 10^{-3} m^2;$$

Total power loss in two inductors $P_{inductor} = 2(P_{rad} + P_{conv})A_s = 3.2W$.

3. Mosfet

Thermal resistance of the mosfet $R_{th,j-a} = 60K/W$;

Temperature rise of the mosfet $\theta = T_{mosfet,K} - T_{room,K} = 21K$;

Total power loss in two mosfets $P_{mosfet} = 2\theta / R_{th,j-a} = 0.7W$.

4. Diode

Thermal resistance of the diode $R_{th,j-a} = 60K/W$;

Temperature rise of the diode $\theta = T_{diode,K} - T_{room,K} = 7K$;

Total power loss in four diodes $P_{diode} = 4\theta / R_{th,j-a} = 0.5W$.

5. Zener

Thermal resistance of the zener $R_{th,j-a} = 60K/W$;

Temperature rise of the zener $\theta = T_{zener,K} - T_{room,K} = 60K$;

Total power loss in two zeners $P_{zener} = 2\theta / R_{th,j-a} = 2.0W$.

A6.2 Power Loss Breakdown for the Converter with a Coaxial Matrix Transformer

The recorded equilibrium temperatures of the magnetic components in the converter are listed in Table A6.2.

Temperature	Room	Transformer	Inductor
T_C (ºC)	24	34	32
T_K (K)	297	307	305

Table A6.2 Equilibrium Temperatures

1. Transformer

   (a) Rate of heat dissipation by radiation (P_{rad})

   Emissivity of the transformer surface $E = 0.95$;

   Rate of heat dissipation by radiation

   $$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T^4_{transformer,K} - T^4_{room,K}\right) = 59.4W/m^2.$$

   (b) Rate of heat dissipation by convection (P_{conv})

   Temperature rise of the transformer $\theta = T_{transformer,K} - T_{room,K} = 10K$;

   Horizontal dimension of the transformer $d_{hor} = 35.0mm$;

   Vertical dimension of the transformer $d_{vert} = 34.6mm$;

   Effective dimension of the transformer $d = \dfrac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 17.4mm$;

   Rate of heat dissipation by convection $P_{conv} = 6.3\dfrac{\theta^{1.25}}{d^{0.25}} = 54.9W/m^2$.

(c) Total power loss in the transformers ($P_{transformer}$)

Total transformer surface area

$$A_s = 4 \times 35.0mm \times 34.6mm + 2 \times (35.0mm)^2 = 7 \times 10^{-3} m^2;$$

Total power loss in five transformers $P_{transformer} = 5(P_{rad} + P_{conv})A_s = 4.0W$.

2. Inductor

(a) Rate of heat dissipation by radiation (P_{rad})

Emissivity of the inductor surface $E = 0.95$;

Rate of heat dissipation by radiation

$$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T_{inductor,K}^4 - T_{room,K}^4\right) = 47.0W / m^2.$$

(b) Rate of heat dissipation by convection (P_{conv})

Temperature rise of the inductor $\theta = T_{inductor,K} - T_{room,K} = 8K$;

Horizontal dimension of the inductor $d_{hor} = 34.8mm$;

Vertical dimension of the inductor $d_{vert} = 29.0mm$;

Effective dimension of the inductor $d = \dfrac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 15.8mm$;

Rate of heat dissipation by convection $P_{conv} = 6.3\dfrac{\theta^{1.25}}{d^{0.25}} = 42.5W / m^2$.

(c) Total power loss in the inductors ($P_{inductor}$)

Total inductor surface area

$$A_s = 4 \times 34.8mm \times 29.0mm + 2 \times (34.8mm)^2 = 7 \times 10^{-3} m^2;$$

Total power loss in two inductors $P_{inductor} = 2(P_{rad} + P_{conv})A_s = 1.3W$.

3. Mosfet

Switch duty cycle $D = 0.5$;

Input current $I_s = 5.48A$;

RMS current in four mosfets on each side $I_{mosfet,rms} = I_s\sqrt{D} = 3.87A$;

Mosfet forward resistance $R_{DS(on)} = 0.1\Omega$;

Conduction loss in eight mosfets $P_{conduction} = 2I_{mosfet,rms}^2\left(R_{DS(on)}/4\right) = 0.7W$.

Switching frequency $f_s = 125kHz$;

Current rise time during turn on $t_r = 50ns$;

Drain source voltage before turn on $V_{ds,off1} = 40V$;

Current fall time during turn off $t_f = 90ns$;

Drain source voltage after turn off $V_{ds,off2} = 50V$;

Switching loss in eight mosfets

$$P_{switching} = 2\times\frac{1}{2}\cdot f_s\cdot I_s/2\left(V_{ds,off1}t_r + V_{ds,off2}t_f\right) = 2.2W;$$

Total power loss in eight mosfets $P_{mosfet} = P_{conduction} + P_{switching} = 2.9W$.

4. Diode

Diode forward current $I_{diode} = \frac{89.76W/5}{34V} = 0.53A$;

Diode forward voltage drop $V_F = 0.75V$;

Total power loss in ten diodes $P_{diode} = 10\times\frac{1}{2}I_{diode}V_F = 2.0W$.

A6.3 Power Loss Breakdown for the Resonant Converter

The recorded equilibrium temperatures of the magnetic components in the converter are listed in Table A6.3.

Temperature	Room	Transformer	Inductors L_1 and L_2	Resonant Inductor L_r
T_C (ºC)	23	64	38	46
T_K (K)	296	337	311	319

Table A6.3 Equilibrium Temperatures

1. Transformer

   (a) Rate of heat dissipation by radiation (P_{rad})

   Emissivity of the transformer surface $E = 0.95$;

   Rate of heat dissipation by radiation

   $$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T_{transformer,K}^4 - T_{room,K}^4\right) = 281.2W/m^2.$$

   (b) Rate of heat dissipation by convection (P_{conv})

   Temperature rise of the transformer $\theta = T_{transformer,K} - T_{room,K} = 41K$;

   Horizontal dimension of the transformer $d_{hor} = 30.6mm$;

   Vertical dimension of the transformer $d_{vert} = 31.6mm$;

   Effective dimension of the transformer $d = \frac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 15.5mm$;

   Rate of heat dissipation by convection $P_{conv} = 6.3\frac{\theta^{1.25}}{d^{0.25}} = 329.4W/m^2$.

   (c) Total power loss in the transformer ($P_{transformer}$)

Total transformer surface area

$$A_s = 4 \times 30.6mm \times 31.6mm + 2 \times (30.6mm)^2 = 6 \times 10^{-3} m^2 ;$$

Total power loss in the transformer $P_{transformer} = (P_{rad} + P_{conv}) A_s = 3.7W$.

2. Inductors L_1 and L_2

(a) Rate of heat dissipation by radiation (P_{rad})

Emissivity of the inductor surface $E = 0.95$;

Rate of heat dissipation by radiation

$$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T^4_{inductor,K} - T^4_{room,K}\right) = 90.4W / m^2 .$$

(b) Rate of heat dissipation by convection (P_{conv})

Temperature rise of the inductor $\theta = T_{inductor,K} - T_{room,K} = 15K$;

Horizontal dimension of the inductor $d_{hor} = 24.7mm$;

Vertical dimension of the inductor $d_{vert} = 18.7mm$;

Effective dimension of the inductor $d = \dfrac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 10.6mm$;

Rate of heat dissipation by convection $P_{conv} = 6.3 \dfrac{\theta^{1.25}}{d^{0.25}} = 103.1W / m^2$.

(c) Total power loss in the inductors ($P_{inductor,dc}$)

Total inductor surface area

$$A_s = 4 \times 24.7mm \times 18.7mm + 2 \times (24.7mm)^2 = 3 \times 10^{-3} m^2 ;$$

Total power loss in two inductors $P_{inductor,dc} = 2(P_{rad} + P_{conv}) A_s = 1.2W$.

3. Resonant Inductor L_r

(a) Rate of heat dissipation by radiation (P_{rad})

Emissivity of the inductor surface $E = 0.95$;

Rate of heat dissipation by radiation

$$P_{rad} = 5.67 \times 10^{-8} \cdot E\left(T_{inductor,K}^4 - T_{room,K}^4\right) = 144.3W/m^2.$$

(b) Rate of heat dissipation by convection (P_{conv})

Temperature rise of the inductor $\theta = T_{inductor,K} - T_{room,K} = 23K$;

Horizontal dimension of the inductor $d_{hor} = 40.0mm$;

Vertical dimension of the inductor $d_{vert} = 39.6mm$;

Effective dimension of the inductor $d = \dfrac{d_{hor} \cdot d_{vert}}{d_{hor} + d_{vert}} = 19.9mm$;

Rate of heat dissipation by convection $P_{conv} = 6.3\dfrac{\theta^{1.25}}{d^{0.25}} = 150.2W/m^2$.

(c) Total power loss in the resonant inductor ($P_{inductor,ac}$)

Total inductor surface area

$$A_s = 4 \times 40.0mm \times 39.6mm + 2 \times (40.0mm)^2 = 1 \times 10^{-2} m^2;$$

Total power loss in the inductor $P_{inductor,ac} = (P_{rad} + P_{conv})A_s = 2.9W$.

4. Mosfet

Switch duty cycle $D = 0.5$;

Input current $I_s = 4.70A$;

RMS current in two mosfets on each side $I_{mosfet,rms} = I_s\sqrt{D} = 3.32A$;

Mosfet forward resistance $R_{DS(on)} = 0.04\Omega$;

Total power loss in four mosfets

$$P_{mosfet} = P_{conduction} = 2I^2_{mosfet,rms}\left(R_{DS(on)} / 2\right) = 0.4W .$$

5. Diode

   Diode forward current $I_{diode} = \frac{95.97W}{360V} = 0.27A$;

   Diode forward voltage drop $V_F = 1.5V$;

   Total power loss in four diodes $P_{diode} = 4 \times \frac{1}{2} I_{diode} V_F = 0.8W$.

6. Resonant Capacitors

   RMS current in seven resonant capacitors on each side $I_{capacitor} = 1.19A$;

   Dissipation factor of the resonant capacitors $DF = 0.5\%$;

   Resonant capacitor $C = 1.5nF$;

   Switching frequency $f_s = 500kHz$;

   Equivalent series resistance of the resonant capacitors $R_s = \frac{DF}{2\pi f_s C} = 1.06\Omega$;

   Total power loss in fourteen resonant capacitors

   $$P_{capacitor} = 2I^2_{capacitor}\left(R_s / 7\right) = 0.4W .$$

APPENDIX 7. PHOTOS OF THE EXPERIMENTAL CONVERTERS

A7.1 The Experimental Converter with a Coaxial Matrix Transformer

Figure A7.1 shows the photo of the experimental converter with a coaxial matrix transformer. The positions of the key components in the experimental converter are shown in Figure A7.2.

A7.2 The Experimental Resonant Converter

Figure A7.3 shows the photo of the resonant converter. The positions of the key components in the experimental converter are shown in Figure A7.4.

Figure A7.1 Photo of the Experimental Converter with a Coaxial Matrix Transformer

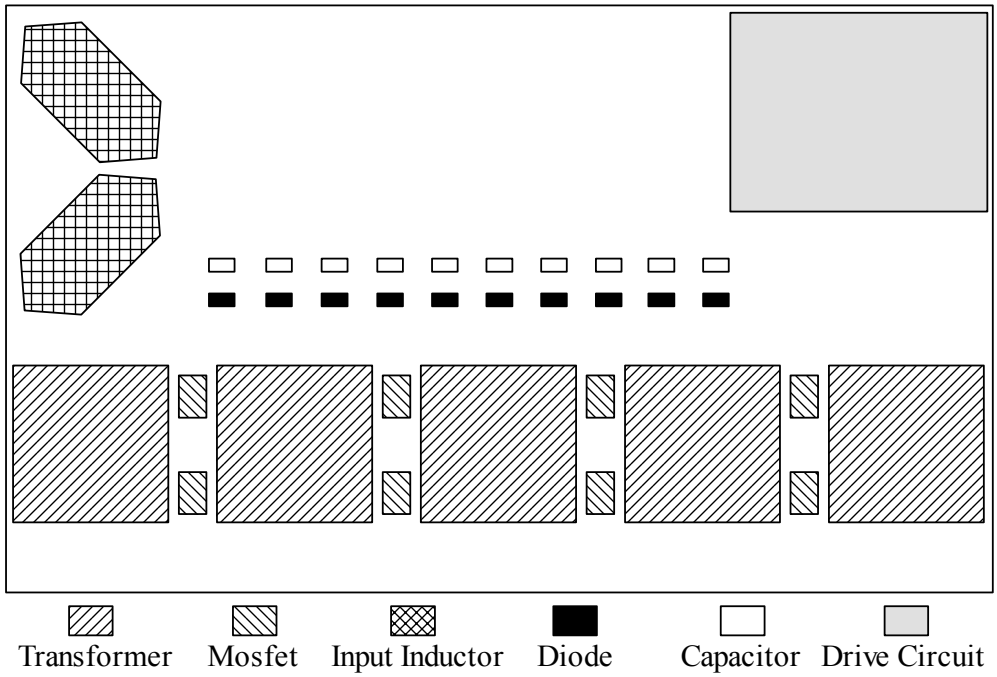


Figure A7.2 Positions of the Key Components

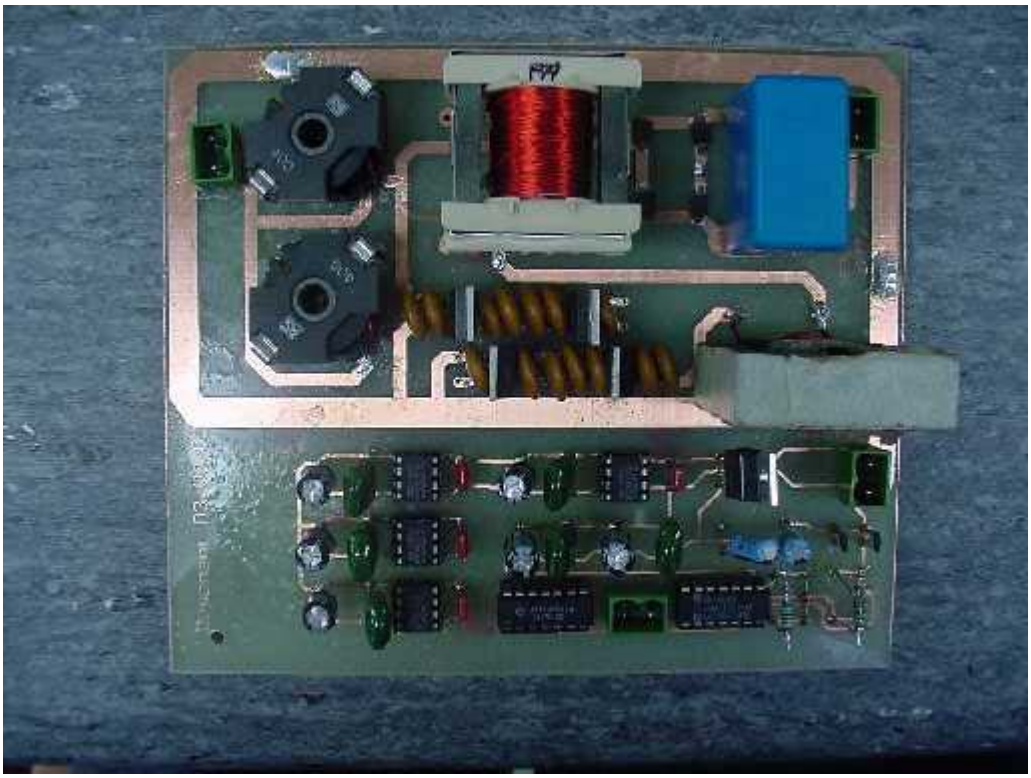


Figure A7.3 Photo of the Resonant Converter

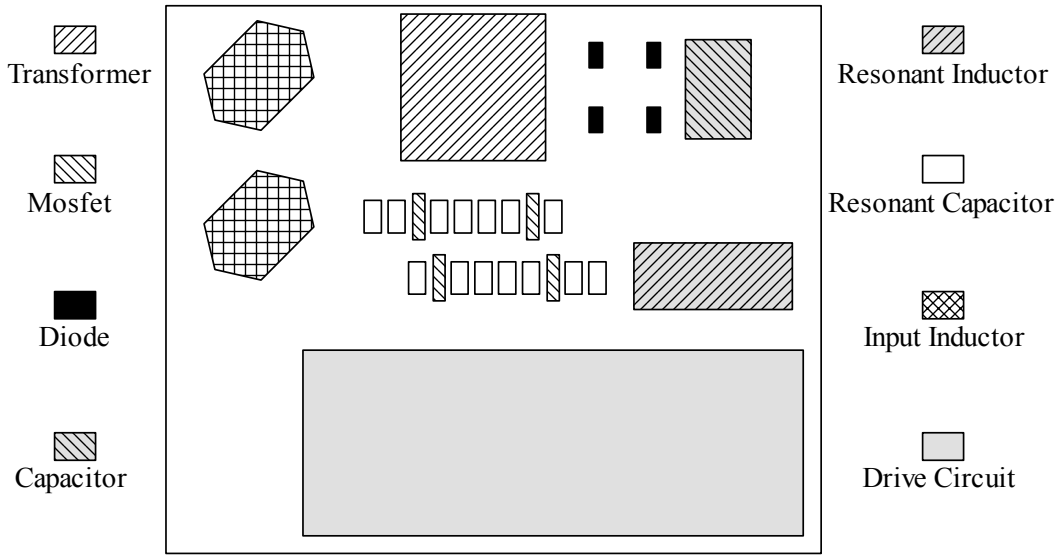


Figure A7.4 Positions of the Key Components

APPENDIX 8. TRANSFORMER OPEN AND SHORT CIRCUIT EXPERIMENTS

Transformer open and short circuit experiments are conducted to verify the transformer core and copper losses respectively. The recorded data and calculation are given below.

A8.1 The Converter with a Coaxial Matrix Transformer

1. Open circuit experiment

   Resonant frequency $f_r = 125kHz$;

   Resonant capacitance $C_r = 0.94nF$;

   RMS voltage across the secondary of the step-up transformer $V_{rms} = 39.5V$;

   Resistance $R_{test} = 32.4\Omega$;

   RMS voltage across the resistor $V_{R,rms} = 0.102V$;

   Total core loss in five transformers $P_{core} = 5\left(V_{rms} \cdot \frac{V_{R,rms}}{R} - \frac{V_{R,rms}^2}{R} \right) = 0.6W$.

2. Short circuit experiment

   RMS voltage across the primary winding of the transformer under test

   $V_{rms} = 0.254V$;

   RMS current in the primary winding of the transformer under test $I_{rms} = 0.5A$;

   Phase angle between the voltage and the current $\phi = 40.5°$;

Total copper loss in five transformers $P_{Cu} = 5V_{rms}I_{rms}\cos\phi = 0.5W$.

A8.2 The Resonant Converter

1. Open circuit experiment

   Self-resonant frequency ***note*** $f_r = 504kHz$;

   Total air gap length of the core $l_g = 0.218mm \times 2 = 0.436mm$;

   RMS voltage across the secondary of the step-up transformer $V_{rms} = 38.2V$;

   Resistance $R_{test} = 24\Omega$;

   RMS voltage across the resistor $V_{R,rms} = 0.396V$;

   Total core loss in the transformer $P_{core} = V_{rms} \cdot \frac{V_{R,rms}}{R} - \frac{V_{R,rms}^2}{R} = 0.62W$.

2. Short circuit experiment

   RMS voltage across the secondary winding of the transformer under test

   $V_{rms} = 6.85V$;

   RMS current in the secondary winding of the transformer under test

   $I_{rms} = 0.264A$;

   Phase angle between the voltage and the current $\phi = 68.8°$;

   Total copper loss in the transformer $P_{Cu} = V_{rms}I_{rms}\cos\phi = 0.7W$.

A8.3 The Resonant Converter with Optimized Components

1. Open circuit experiment

   Self-resonant frequency ***note*** $f_r = 496kHz$;

   Total air gap length of the core $l_g = 0.221mm \times 2 = 0.442mm$;

   RMS voltage across the secondary of the step-up transformer $V_{rms} = 37.8V$;

   Resistance $R_{test} = 24\Omega$;

   RMS voltage across the resistor $V_{R,rms} = 0.215V$;

   Total core loss in the transformer $P_{core} = V_{rms} \cdot \frac{V_{R,rms}}{R} - \frac{V_{R,rms}^2}{R} = 0.34W$.

2. Short Circuit Experiment

   RMS voltage across the secondary winding of the transformer under test

   $V_{rms} = 6.6V$;

   RMS current in the secondary winding of the transformer under test

   $I_{rms} = 0.264A$;

   Phase angle between the voltage and the current $\phi = 65.9°$;

   Total copper loss in the transformer $P_{Cu} = V_{rms} I_{rms} \cos\phi = 0.7W$.

Note: The ungapped transformer was self-resonant below 500kHz due to winding capacitance. It was gapped to achieve resonant frequency of 500kHz.

APPENDIX 9. QUASI-RESONANT CONVERTERS

This appendix lists different switching cell topologies for different types of Quasi-Resonant Converters, [48].

A9.1 Zero-Current Switching Converters

The configurations of the basic switching cells made up of the mosfet, the inductor and the capacitor in different types of ZCS converters are shown in Figure A9.1.

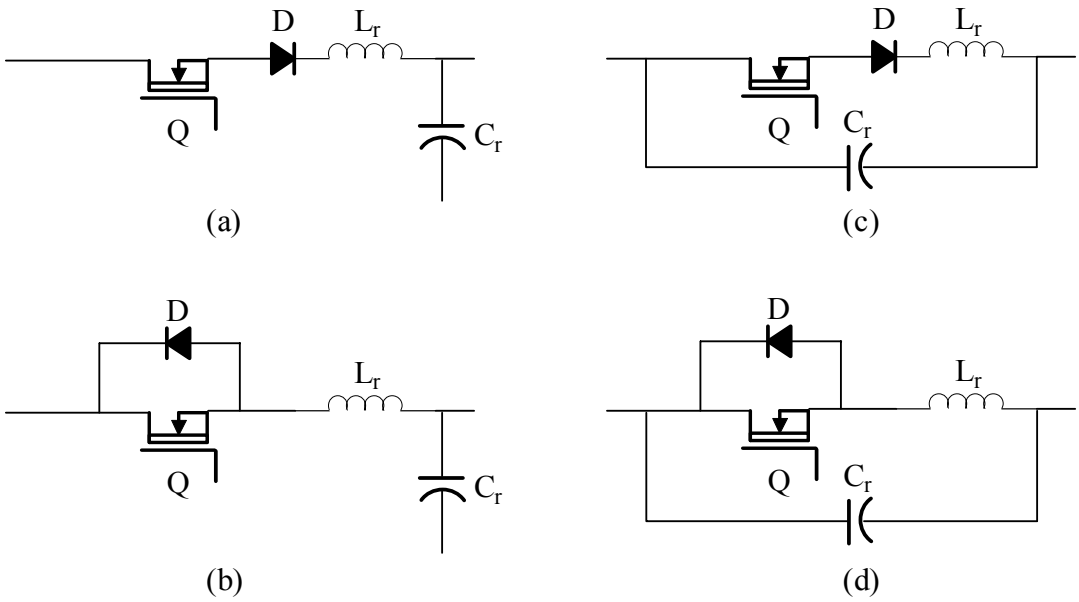


Figure A9.1 Switching Cell in ZCS Converters (a) L-Type Half-Wave (b) L-Type Full-Wave (c) M-Type Half-Wave (d) M-Type Full-Wave

A9.2 Zero-Voltage Switching Converters

The configurations of the basic switching cells made up of the mosfet, the inductor and the capacitor in different types of ZVS converters are shown in Figure A9.2.

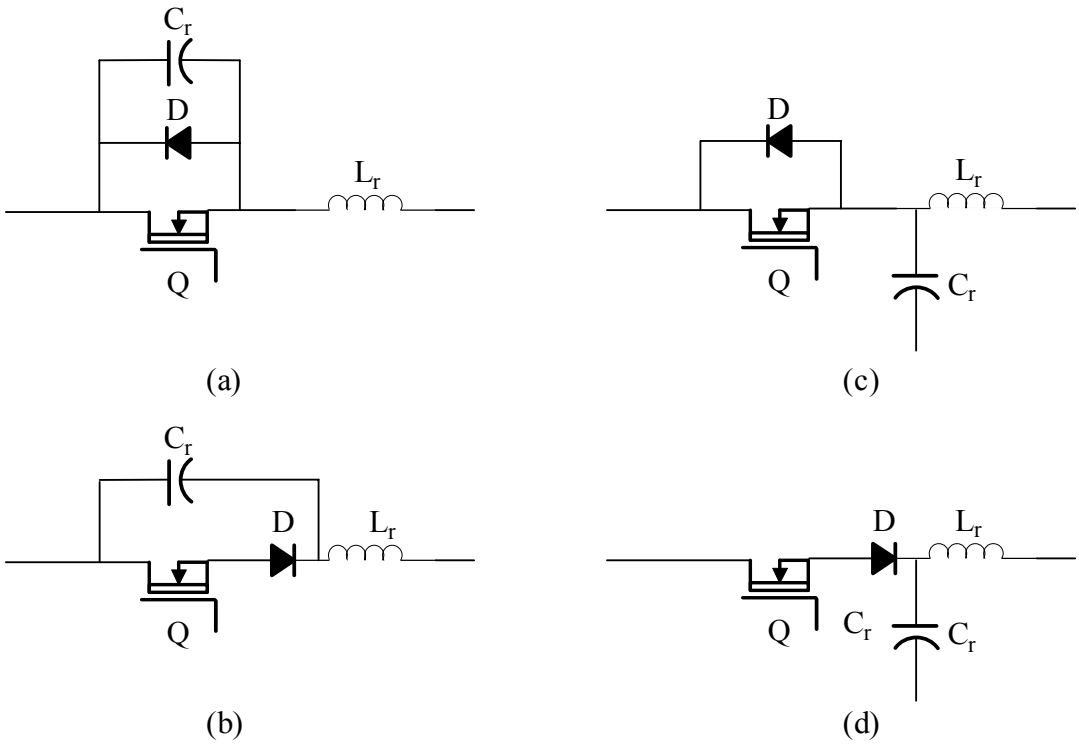


Figure A9.2 Switching Cell in ZVS Converters (a) L-Type Half-Wave (b) L-Type Full-Wave (c) M-Type Half-Wave (d) M-Type Full-Wave