8. CONCLUSIONS

This thesis concentrated on the development of the converter topologies based on the two-inductor boost converter for MIC applications. It has presented a broad range of new contributions to our understanding of the two-inductor boost converter and builds significantly upon the author's earlier Master of Engineering study.

Chapter 2 classified the MIC implementations with high frequency transformers into three topologies and provided a review of the existing literature on the individual topologies. Amongst the three possible MIC topologies, the MIC implementations with an unfolding stage have drawn significant interest and the reasons are:

- Two separate dc-dc and dc-ac conversion stages make the design and the control relatively simple.
- The dc-ac conversion stage operates at low frequency and this avoids the high switching losses.

Chapter 3 discussed the power balance issue in the MIC design. In order to deal with the 100-Hz power ripple in MIC implementations, capacitive energy storage is most frequently used and it can be located at the converter input, dc link or output as a second phase associated with the load. Then a review of the recent literature on the two-inductor boost converter was presented. Also, different arrangements of the two-inductor boost converter including the two-inductor boost converters with a

PWM inverter, an unfolder and a frequency changer were respectively demonstrated for the individual MIC topologies.

Chapter 4 presented a detailed analysis of the ZVS two-inductor boost converter. Under variable frequency control, the ZVS two-inductor boost converter is able to achieve a maximum to minimum output voltage ratio of 2.3 by varying the three circuit parameters including the load factor, the timing factor and the delay angle while maintaining the resonant condition. The ZVS two-inductor boost converter with the voltage clamp was also analysed in detail and a larger maximum to minimum output voltage ratio of 5.3 could be obtained in this converter without excessive switch voltage stresses. Both of the design equations and the control functions were established for the two resonant two-inductor boost converters.

If the ZVS two-inductor boost converter is required to operate under a fixed load condition, different operating conditions exist, which require different combinations of the three circuit parameters as mentioned above and the three key converter design parameters including the resonant inductance and capacitance and the transformer turns ratio. It has been shown that the power losses in the MOSFETs, the resonant inductor and capacitors vary under different operating conditions. These power loss terms as well as the total variable power loss can be drawn as surfaces using the numerical analysis in MATLAB and the operating point with the minimised total power loss can be easily identified.

Chapter 5 provided a detailed analysis of the magnetic integration solutions in the two-inductor boost converter, which aim to integrate the three separate magnetic components and achieve an overall compact design. This chapter systematically developed four integrated magnetic structures using both of the magnetic core integration and the winding integration methods. A detailed analysis of the equivalent input and transformer magnetising inductances, the dc gain, the dc and ac flux densities and the current ripples in the individual windings of the hard-switched two-inductor boost converter with four integrated magnetic structures was also provided. It has been shown that among the four integrated magnetic structures, Structure A has the lowest transformer leakage inductance, Structure B has the lowest number of copper winding components and Structures C and D have the lowest ac flux densities in the centre core leg therefore the lowest core loss.

The ZVS two-inductor boost converter with Structure B magnetic integration was also analysed in detail. In this converter, the four magnetic cores and the five copper windings required by the two input inductors, the resonant inductor and the transformer are integrated into one magnetic core with three copper windings. With the magnetic integration technique, the component count is significantly reduced and this results in a more compact converter design with possible higher efficiency. Finally, a 40-W prototype converter has been developed and achieved 93% efficiency.

Chapter 6 developed the hard-switched and the soft-switched current fed two-inductor boost converters. These two converters are both three-stage converters

including the buck, the boost and the inversion stages. In the buck stage, a two-phase synchronous buck converter is modulated to produce a rectified sinusoidal current and interfaced with the two-inductor boost cell through an IPT. As the boost stage converter produces a fixed dc gain, the rectified sinusoidal voltage is generated at the output and this reduces the following inverter to an unfolder with simple square-wave control.

In the hard-switched current fed two-inductor boost converter, non-dissipative snubbers are employed to control the switch voltage stress and recover part of the energy trapped in the snubber circuit back to the supply. The four operation modes in the snubber circuit under different buck stage MOSFET duty ratios were thoroughly studied. Structure A magnetic integration, which has been discussed in Chapter 5 and the silicon carbide rectifiers, which have high reverse breakdown voltage ratings and the near zero reverse recovery time are also used in the two-inductor boost cell to minimise the converter size and power loss.

In the soft-switched current fed two-inductor boost converter, a resonant transition gate drive circuit is developed for the two MOSFETs in the boost cell to reduce the drive power loss, which will otherwise become significant under high switching frequency operation if a conventional gate drive circuit is used. The two-inductor boost cell is also designed to operate at the optimised operating point with the minimised total variable power loss as discussed in Chapter 4.

In the unfolder for both converters, the electrically isolated optical MOSFET drivers are used to achieve a simple control circuit design. The hard-switched and the soft-switched current fed two-inductor boost converters have respectively achieved 92% and 91% efficiency.

Chapter 7 presented the two-inductor boost converter with a frequency changer. In this two-stage converter, no dc link exists in the power conversion process. The rectification stage of the two-inductor boost converter is replaced by a frequency changer, which converts the high frequency ac current directly to the ac voltage of the grid frequency. Compared with the MIC implementations with the constant or the variable dc link, this topology is simpler and has a potential for size reduction. A small non-polarised capacitor is also employed in the converter in combination with the resistive load to achieve the constant power output and the large electrolytic capacitor, which is normally used to deal with the 100-Hz power ripple, can be avoided. It has been shown that in the practical implementation of this converter, a diode is required to be in series with the low-voltage primary side MOSFET to provide the reverse voltage blocking. The practical implementation of the hard-switched converter and the development of the soft-switched converter are both areas of future research.

Another future research area is the implementation of the digital control for the converter topologies presented in this thesis, which is expected to result in the reductions of the overall converter size and control power loss. It is also clear that the resonant converter understandings developed in this thesis can be readily

extended to the hard-switched variations of the two-inductor boost converters that have been recently proposed by other researchers. This is a promising avenue for future research.